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1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.

2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.

3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

Q

起点主板维修网

www.qdzbwx.com

SCHEM, ANGEL_ISLAND, MLB, K17

Rev.A 02/23/10

REV

ECN

DESCRIPTION OF REVISION

CK APPD

DATE

2009-05-19

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PROJECT SPECIFIC CONNS

Front Flex Support

Sync

K20A_MLB

K20A_MLB

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K17_WFERRY

K17_REF

(MASTER)

K17_REF

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K17_REF

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K20A_MLB

Date

04/01/2008

03/26/2009

03/26/2009

03/26/2009

06/09/2009

06/17/2009

(MASTER)

06/17/2009

06/09/2009

10/14/2009

04/29/2009

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LCD Backlight Support

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06/17/2009

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ALIASES

RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8503	1	SCHEM,ANGEL_ISLAND,MLB,K17	SCH	CRITICAL	
820-2849	1	PCBF,ANGEL_ISLAND,MLB,K17	PCB	CRITICAL	

DRAWING

TITLE=MLB

ABBREV=DRAWING

LAST_MODIFIED=Thu Feb 23 21:52:40 2010

SCHEM, TREASURE_ISLAND, MLB, K17

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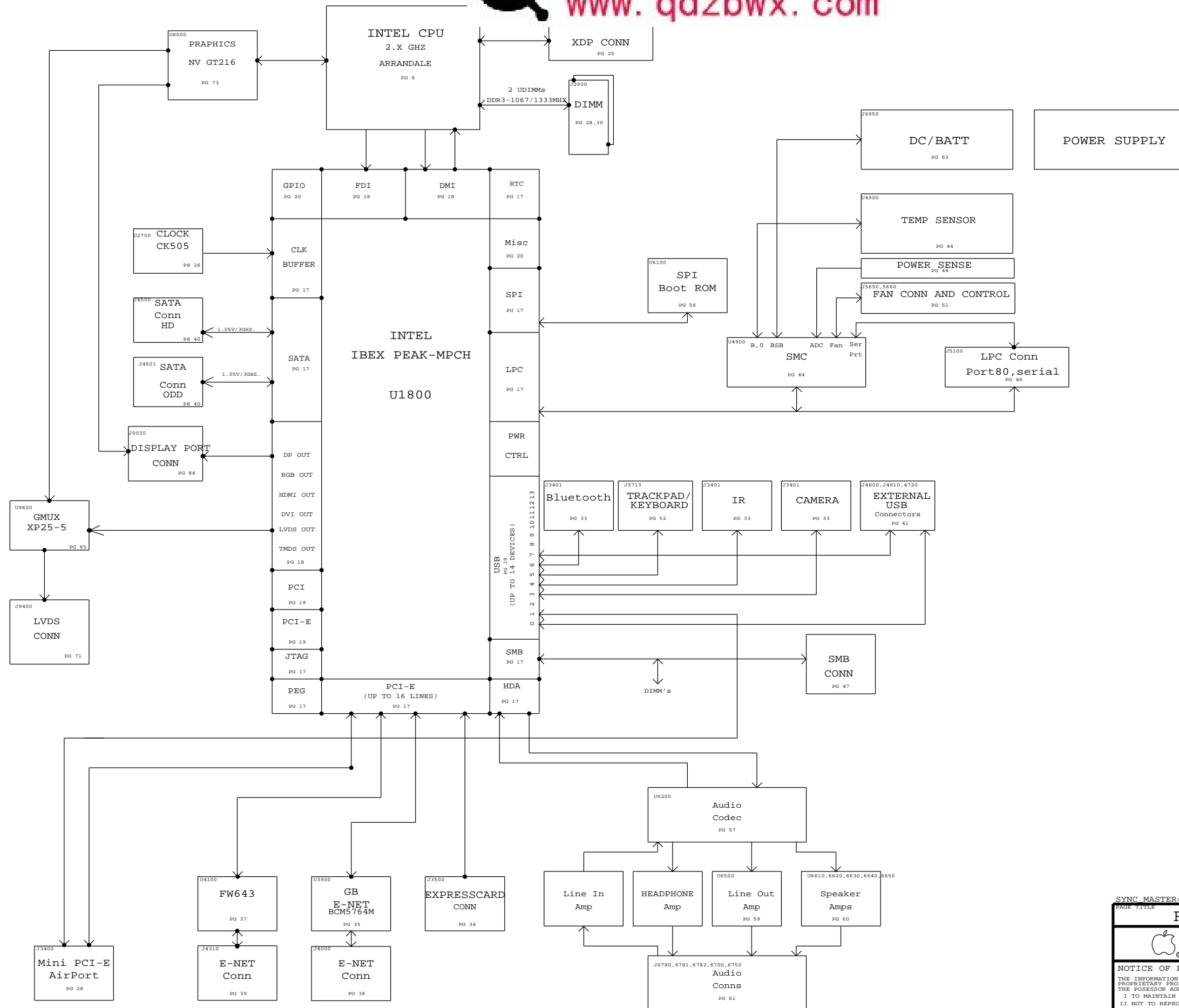
4


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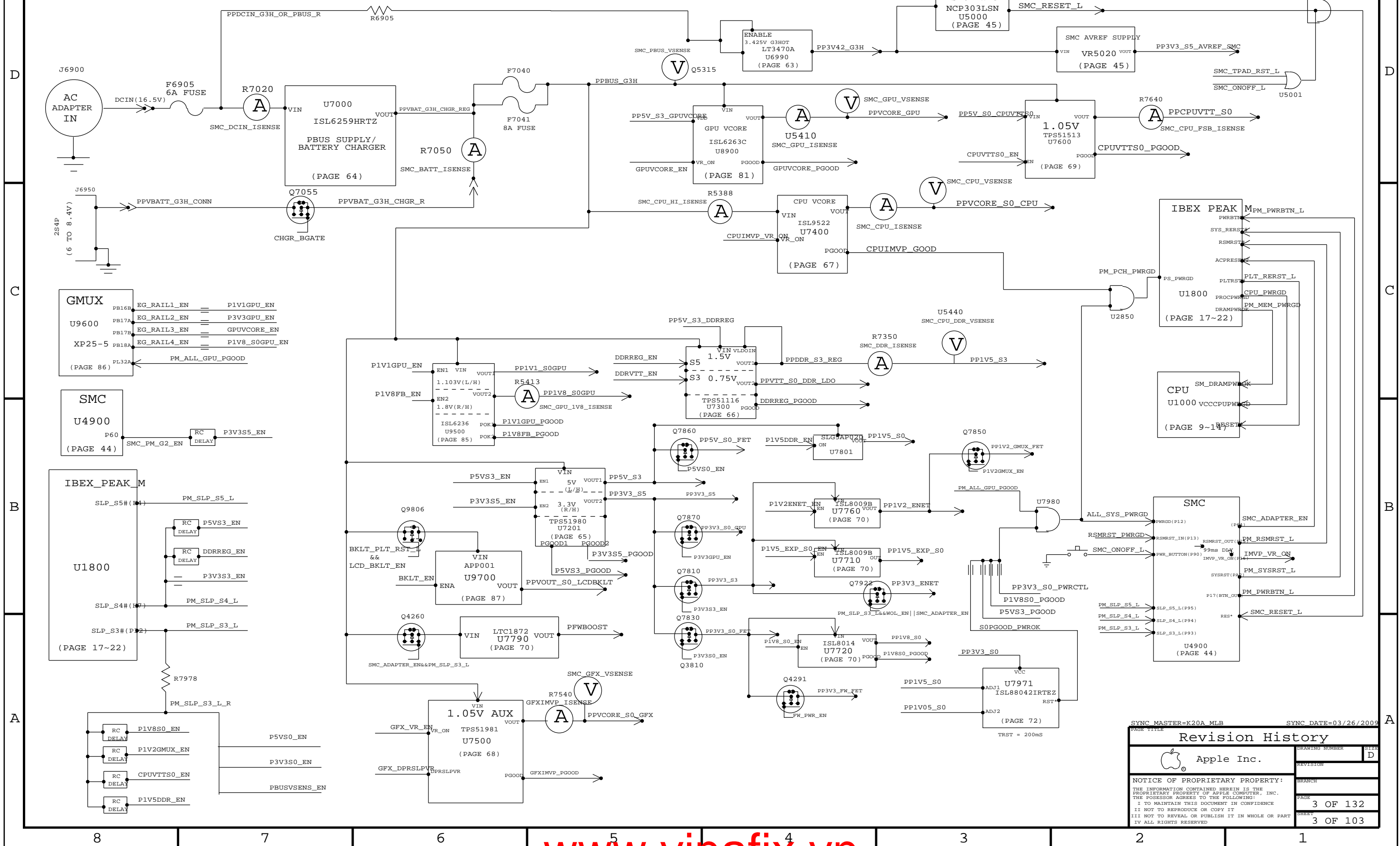
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K17 POWER SYSTEM ARCHITECTURE





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(For changes prior to Rev. A, refer to earlier schematics)
Rev. A:

02/23/10
MLB_TI_IMVP65
csa. 5 Added K17_PVT BOM group
csa. 74 Updated Symbol for U7400; new VPN is TPS51983
csa. 121 Changed ARB_ONLY sense Rs to XWs

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BOM Variants			
BOM NUMBER	BOM NAME	BOM OPTIONS	
639-0973	PCBA, 2.53GHZ, 512SAM_VRAM, K17	K17_COMMON, CPU_2_53GHZ, FB_512_SAMSUNG, EEEE_DCMV, K17_PVT	
639-0971	PCBA, 2.53GHZ, 512HYN_VRAM, K17	K17_COMMON, CPU_2_53GHZ, FB_512_HYNIX, EEEE_DCMR, K17_PVT	
639-0972	PCBA, 2.66GHZ, 512SAM_VRAM, K17	K17_COMMON, CPU_2_66GHZ, FB_512_SAMSUNG, EEEE_DCMT, K17_PVT	
639-0970	PCBA, 2.66GHZ, 512HYN_VRAM, K17	K17_COMMON, CPU_2_66GHZ, FB_512_HYNIX, EEEE_DCMQ, K17_PVT	
085-1425	K17 MLB DEVELOPMENT	K17_DEVEL_ENG	

138S0603	138S0602		ALL	Murata alt to Samsung
157S0058	157S0055		ALL	Delta alt to TDK Magnetics
152S0896	152S0518		ALL	MAG LAYERS ALT TO CYWTRC
152S0915	152S0796		ALL	MAG LAYERS ALT TO CYNTEC
155S0457	155S0329		ALL	MAG LAYERS ALT TO MURATA
516S0806	516S0805		ALL	FOXCONN ALT TO MOLEX
138S0612	138S0602		ALL	Taiyo Yuden alt to Samsung
353S2805	353S2603		ALL	Fairchild 8 in alt to 6 in wafer
127S0111	127S0060		ALL	Robm alt to Kemet
128S0299	128S0218		ALL	NEC/TOKIN alt to Sanyo
337S3808	337S3839		ALL	GT216 A02 alt to A03 part
376S0887	376S0749		ALL	Fairchild alt to Vishay

K17 BOM GROUPS

BOM GROUP	BOM OPTIONS
K17_COMMON	ALTERNATE, COMMON, K17_COMMON1, K17_COMMON2, K17_PROGPARTS
K17_COMMON1	BCM5764M, DCI, GMUX_VSYNC, CPUPOC_IMAX_40_50, PCH_NAND_3V3, CPUMEM_S0, EXT_HP_AMP, VFRO_SLP3, SMC_DEBUG_YES, DPMUX_EN_PLD, FB1V35, USBHUB_2061
K17_COMMON2	GPUVID_0P90V, BKLT_PWR_PBUS, DP_ESD, DP_CA_DET_EG_PLD, SMC_EXCARD_NOT, GPU_SS_INT, RDRV_8515_A2, GMUXPLL_3V3, HUB1_2NONREM, HUB2_2NONREM, RAIL_MON
K17_DEVEL_ENG	ARB_ONLY, CALPELLA_XDP, DEBUG_ADC, LPCPLUS, VREFMRGN, GMUX_JTAG_CONN, EFI_DEBUG, BMON_ENG, SMC_OSC_YES
K17_PROGPARTS	GMUX_PROG, BOOTROM_PROG, SMC_PROG, TPAD_PROG
K17_PVT	BMON_PROD, VREFMRGN_NOT, XDP, XDP_NORMAL, XDP_CPU_BPM


BOM GROUP	BOM OPTIONS
FB_512_SAMSUNG	VRAM4, VRAM_512_SAMSUNG
FB_512_HYNIX	VRAM4, VRAM_512_HYNIX
CALPELLA_XDP	XDP, XDP_CONN, XDP_CPU_BPM, XDP_NORMAL, XDP_PCH

Bar Code Labels / EEEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEEE_DCMQ]	CRITICAL	EEEE_DCMQ
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEEE_DCMR]	CRITICAL	EEEE_DCMR
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEEE_DCMT]	CRITICAL	EEEE_DCMT
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEEE_DCMV]	CRITICAL	EEEE_DCMV

Module Parts

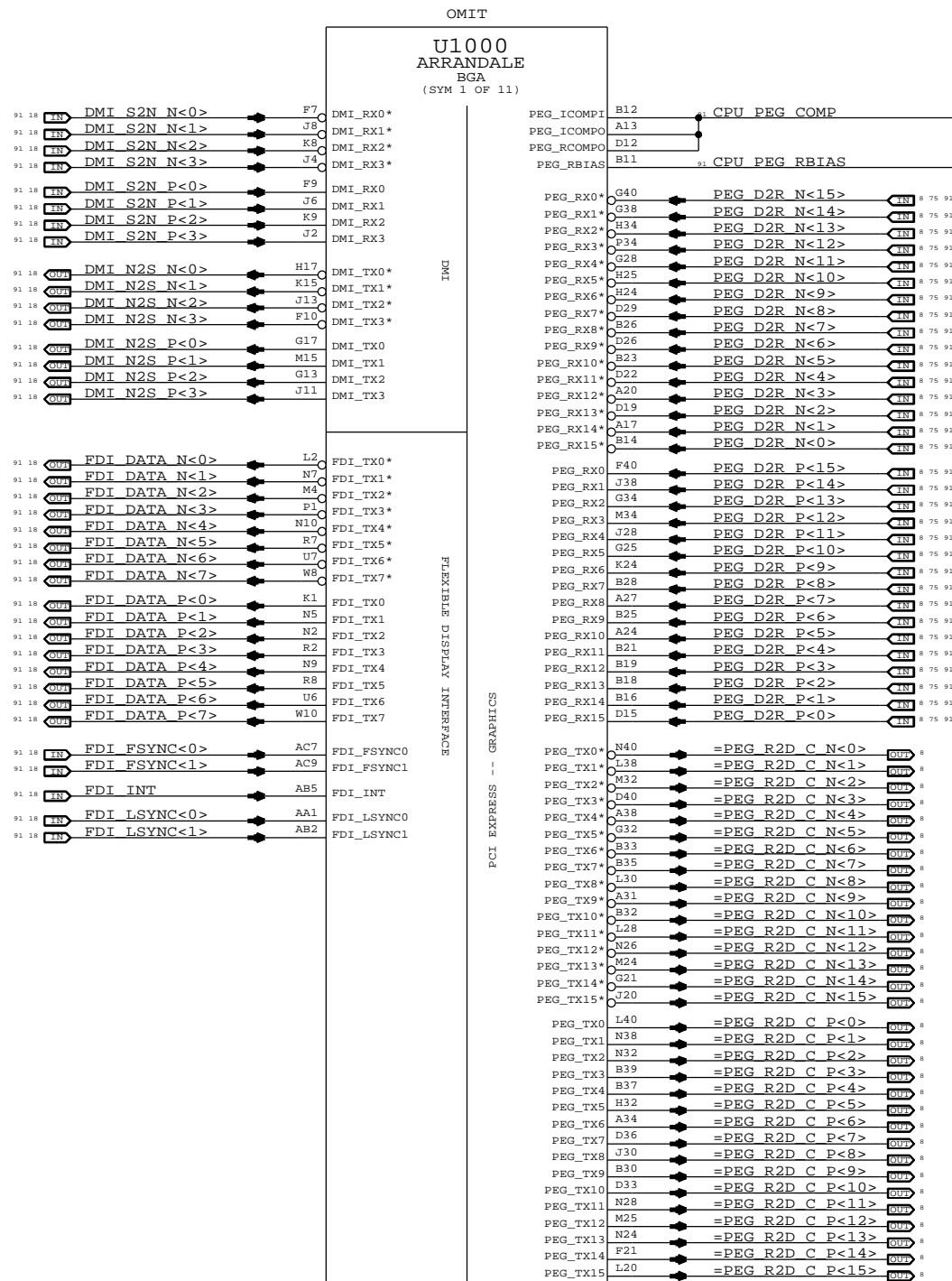
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3847	1	ARD, SLBPF, PRQ, 2.53, 35W, C2, 3M, BGA	U1000	CRITICAL	CPU_2_53GHZ
337S3848	1	ARD, SLBPF, PRQ, 2.66, 35W, C2, 4M, BGA	U1000	CRITICAL	CPU_2_66GHZ
337S3846	1	ARD, SLBNA, PRQ, 2.40, 35W, C2, 3M, BGA	U1000	CRITICAL	CPU_2_4GHZ
337S3849	1	IBEX (HM55), SLGZS, PRQ, B3	U1800	CRITICAL	
337S3839	1	IC, GPU, NV GT216 LP++, 969BGA, 40NM, A03	U8000	CRITICAL	
343S0493	1	IC, ASIC, BCM5764M, ENET CONTROLLER, 8x8, 64 QFN	U3900	CRITICAL	BCM5764M
338S0753	1	IC, FW643-E, 1394B PHY/OHCI LINK/PCI-E, 12	U4100	CRITICAL	
338S0563	1	IC, SMC, HS8/2117, 9MMX9MM, TLP	U4900	CRITICAL	SMC_BLANK
341T0229	1	IC, SMC, K17	U4900	CRITICAL	SMC_PROG
335S0610	1	IC, FLASH, SPI, 32MBIT, 3.3V, 86MHZ, 8-SOP	U6100	CRITICAL	BOOTROM_BLANK
341T0244	1	IC, EFI ROM, K17	U6100	CRITICAL	BOOTROM_PROG
341S2384	1	IR, ENCORE II, CY7C63833-LFXC	U4800	CRITICAL	
341S2616	1	IC, TP PSOC, K17, K18	U5701	CRITICAL	TPAD_PROG
336S0025	1	IC, XP2-5, HF, CPLD, BLANK	U9600	CRITICAL	GMUX_5K_BLANK
341S2568	1	IC, CPLD, LATTICE, 132CSBGA, K17MLB	U9600	CRITICAL	GMUX_PROG
333S0533	4	IC, SDRAM, GDDR3, 32MX32, 10MHZ, D-DIE, 136 FBGA	U8400, U8450, U8500, U8550	CRITICAL	VRAM_512_SAMSUNG
333S0535	4	IC, SDRAM, GDDR3, 32MX32, 900MHZ, TIVA, HF	U8400, U8450, U8500, U8550	CRITICAL	VRAM_512_HYNIX
341S2731	1	IC, 1MBIT, SPI FLASH K17/K18	U3990	CRITICAL	
516S0805	1	CONN, 204P, SOD1MM, SOCKET, DDR3, RAM, NON/SC	J3100	CRITICAL	
197S0350	1	OSC, XTAL, 32.768KHZ, 9-3.6V, 12P SOIC, HF	U5010	CRITICAL	SMC_OSC_YES

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BOM Configuration			
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Embedded DisplayPort
(eDP) pins
(Auburndale only):

eDP_AUX#

NOTE: HPD must be inverted
and level-shifted for
Auburndale (1.05V).

eDP_HPDP#
eDP_AUX

eDP_TX#<3>
eDP_TX#<2>
eDP_TX#<1>
eDP_TX#<0>

eDP_TX#<3>
eDP_TX#<2>
eDP_TX#<1>
eDP_TX#<0>

91 25	CFG0	(IPU)
91 25	CFG1	(IPU)
91 25	CFG2	(IPU)
91 25 8	CFG3	(IPU)
91 25	CFG4	(IPU)
91 25	CFG5	(IPU)
91 25	CFG6	(IPU)
91 25	CFG7	(IPU)
91 25	CFG8	(IPU)
91 25	CFG9	(IPU)
91 25	CFG10	(IPU)
91 25	CFG11	(IPU)
91 25	CFG12	(IPU)
91 25	CFG13	(IPU)
91 25	CFG14	(IPU)
91 25	CFG15	(IPU)
91 25	CFG16	(IPU)
91 25	CFG17	(IPU)

TP CPU RSVD TP0	AU1	RSVD_TP0
TP CPU RSVD<15>	T4	RSVD15
TP CPU RSVD<16>	T2	RSVD16
TP CPU RSVD<17>	U1	RSVD17
TP CPU RSVD<18>	V2	RSVD18
TP CPU RSVD<19>	AV71	RSVD19
TP CPU RSVD<20>	AW70	RSVD20
TP CPU RSVD<21>	AY69	RSVD21
TP CPU RSVD<22>	BB69	RSVD22
TP CPU RSVD<23>	D8	RSVD23
TP CPU RSVD<24>	B7	RSVD24
TP CPU RSVD<26>	A10	RSVD26
TP CPU RSVD<27>	B9	RSVD27
NC TP CPU RSVD NCTF<7>	C5	RSVD_NCTF7
NC TP CPU RSVD NCTF<8>	A6	RSVD_NCTF8
NC TP CPU RSVD NCTF<6>	E3	RSVD_NCTF6
NC TP CPU RSVD NCTF<5>	F1	RSVD_NCTF5

CFG0: PCIe Configuration Select 1 = Single PEG 0 = Bifurcation Enabled
CFG3: PCIe Lane Reversal 1 = Normal Operation 0 = Lanes Reversed
CFG4: Display Port Presence 1 = eDP Disabled 0 = Embedded Display Port Enabled

WF: RSVD nets with arrows have offpage marks on CRB schematic.
WF: RSVD nets with red wires have 0-ohm resistors to GND in CRB schematic.

RESERVED

RSVD32	W66	NC TP CPU RSVD<32>
RSVD33	W64	NC TP CPU RSVD<33>
RSVD34	AC69	NC TP CPU RSVD<34>
RSVD35	AC71	NC TP CPU RSVD<35>
RSVD36	AA71	NC TP CPU RSVD<36>
RSVD37	AA69	NC TP CPU RSVD<37>
RSVD38	R66	NC TP CPU RSVD<38>
RSVD39	R64	NC TP CPU RSVD<39>
RSVD_NCTF3	BT5	NC TP CPU RSVD<40>
RSVD_NCTF4	BR5	NC TP CPU RSVD<41>
RSVD_NCTF2	BV6	NC TP CPU RSVD<42>
RSVD_NCTF1	BV8	NC TP CPU RSVD<43>
RSVD45	AV69	TP CPU RSVD<45>
RSVD46	AK71	TP CPU RSVD<46>
RSVD47	AN69	TP CPU RSVD<47>
RSVD48	AP66	TP CPU RSVD<48>
RSVD49	AH66	TP CPU RSVD<49>
RSVD50	AK66	TP CPU RSVD<50>
RSVD51	AR71	TP CPU RSVD<51>
RSVD52	AM66	TP CPU RSVD<52>
RSVD53	AK69	TP CPU RSVD<53>
RSVD54	AU71	TP CPU RSVD<54>
RSVD55	AT70	TP CPU RSVD<55>
RSVD56	AR69	TP CPU RSVD<56>
RSVD57	AU69	TP CPU RSVD<57>
RSVD58	AT67	TP CPU RSVD<58>
RSVD_TP2	AP2	TP CPU RSVD<2>
RSVD_TP1	AN7	TP CPU RSVD<1>
RSVD62	AV4	CPU THERMD P
RSVD63	AU2	CPU THERMD N
RSVD64	BE69	TP CPU RSVD<64>
RSVD65	BE71	TP CPU RSVD<65>
DC_TEST_BV71	BV71	CPU TEST BV71 BV69
DC_TEST_BV69	BV69	
DC_TEST_BV68	BV68	TP CPU TEST BV68
DC_TEST_BV5	BV5	TP CPU TEST BV5
DC_TEST_BV3	BV3	CPU TEST BV3 BT3
DC_TEST_BV1	BV1	CPU TEST BV1 BT1
DC_TEST_BT71	BT71	CPU TEST BT71 BT69
DC_TEST_BT69	BT69	
DC_TEST_BT3	BT3	
DC_TEST_BT1	BT1	
DC_TEST_BR71	BR71	TP CPU TEST BR71
DC_TEST_BR1	BR1	TP CPU TEST BR1
DC_TEST_E71	E71	TP CPU TEST E71
DC_TEST_E1	E1	TP CPU TEST E1
DC_TEST_C71	C71	CPU TEST C71 A71
DC_TEST_C69	C69	CPU TEST C69 A69
DC_TEST_C3	C3	TP CPU TEST C3
DC_TEST_A71	A71	
DC_TEST_A69	A69	
DC_TEST_A68	A68	TP CPU TEST A68
DC_TEST_A5	A5	TP CPU TEST A5

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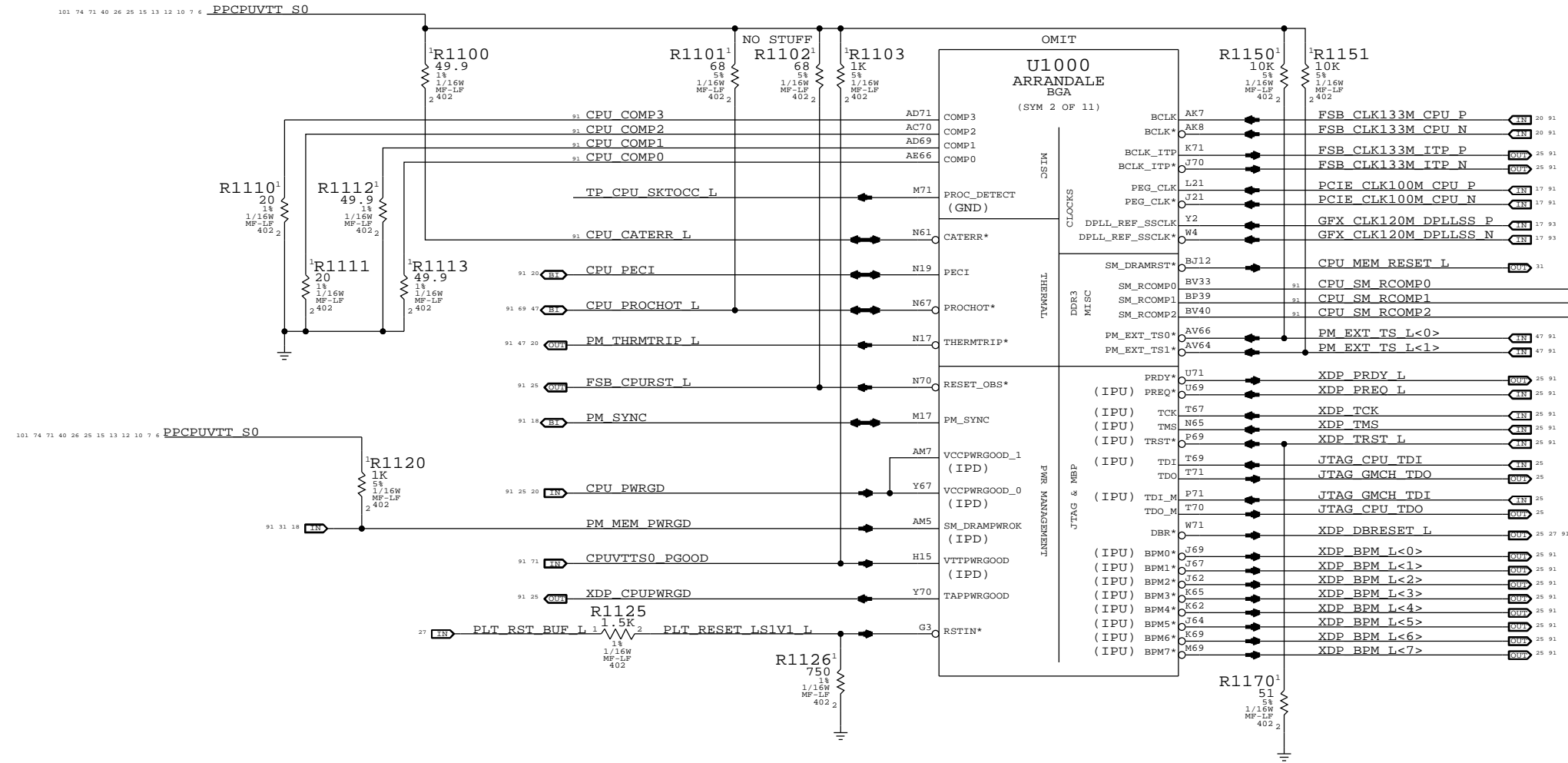
C

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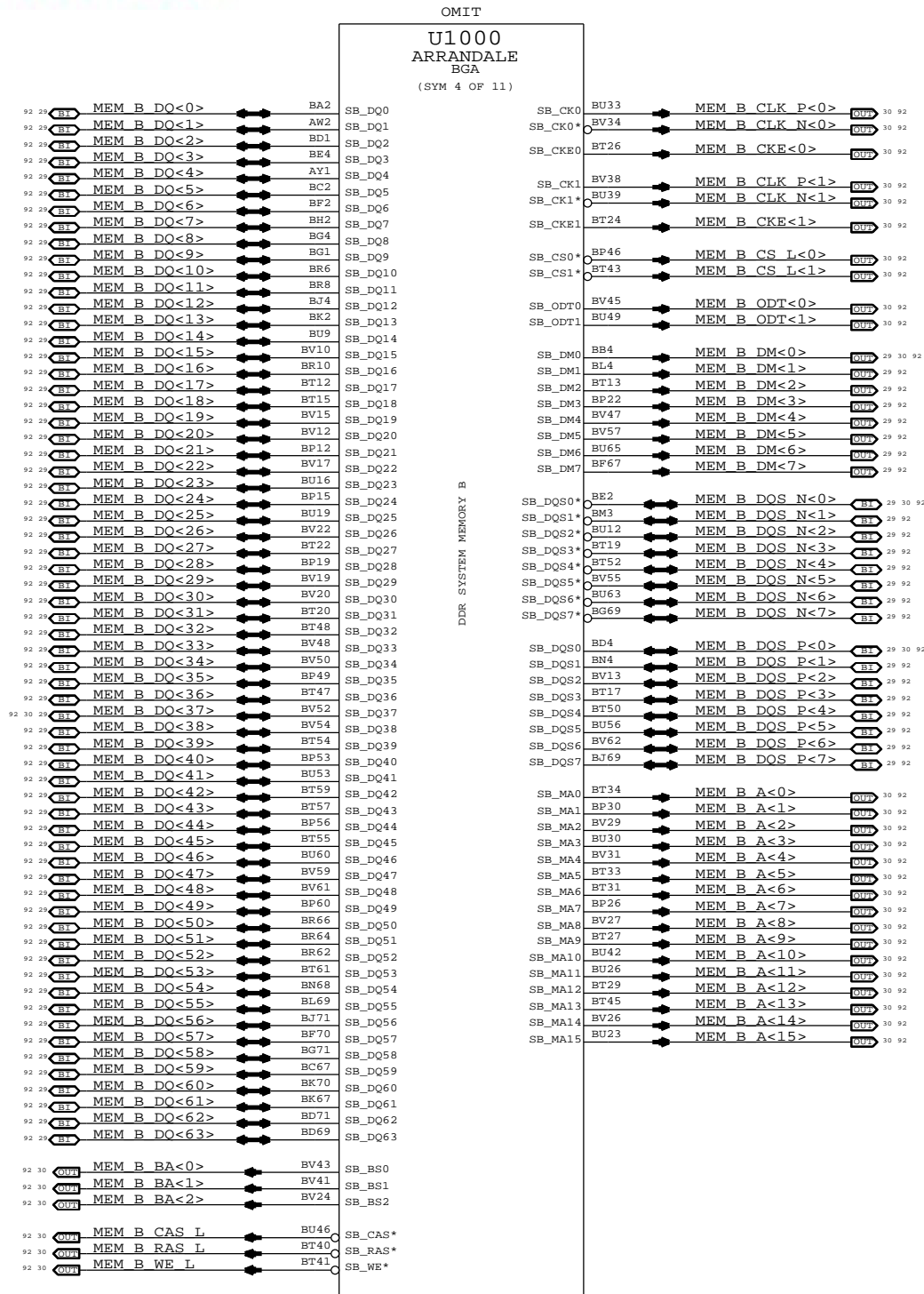
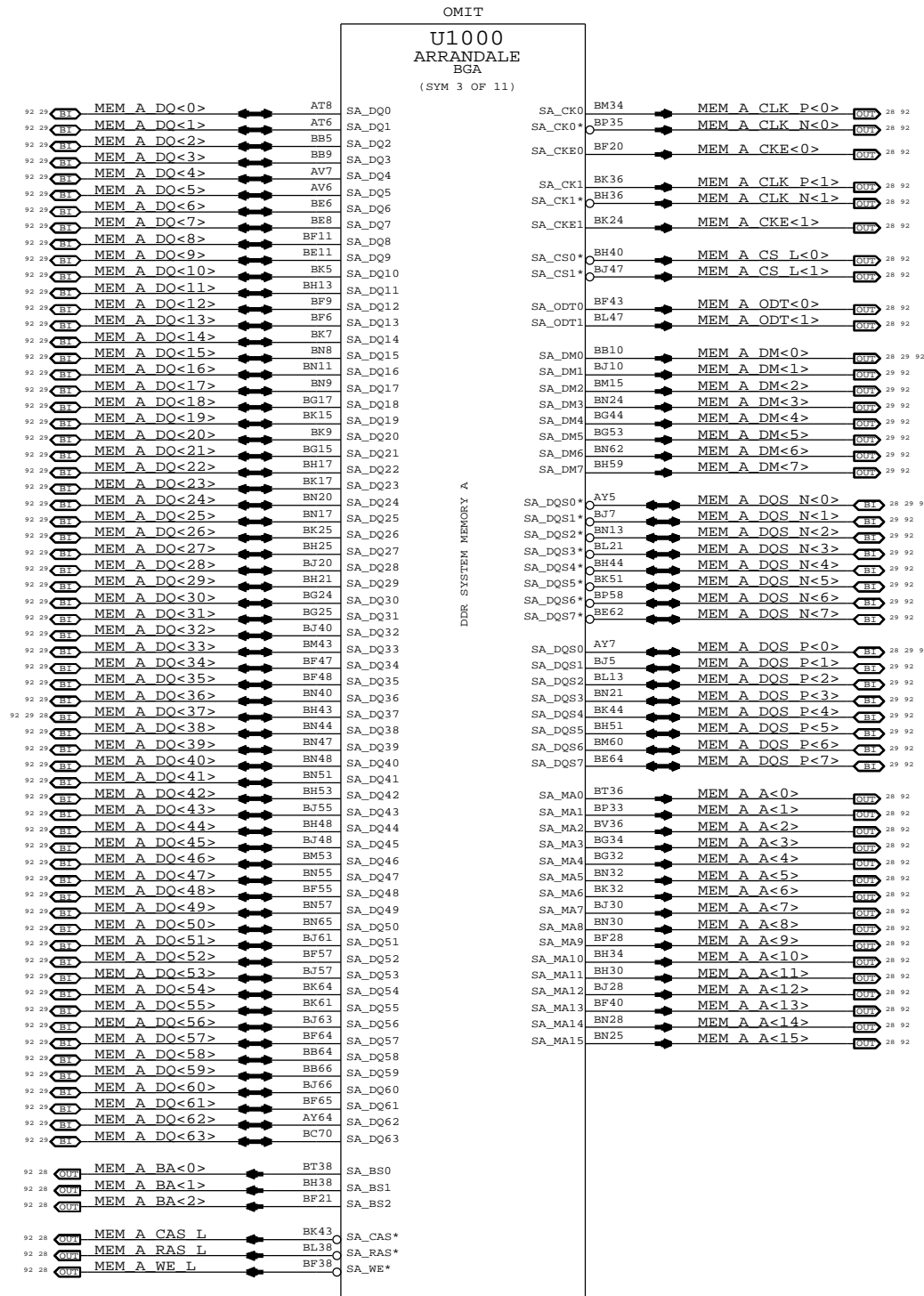
B

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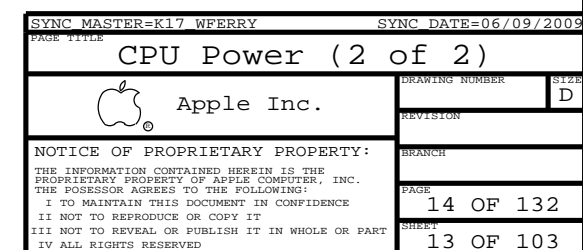
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SYNC MASTER=K18_MLB		SYNC DATE=10/14/2009	
CPU Clock/Misc/JTAG			
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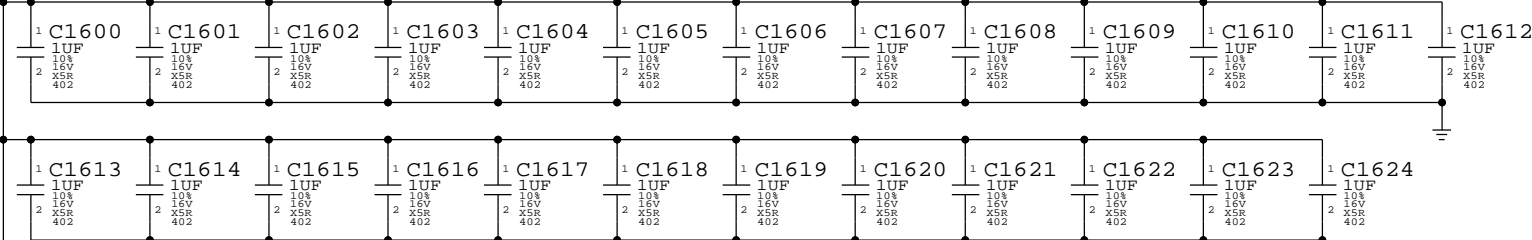


CPU VCore HF and Bulk Decou

3x 470uF 4.5mOhm, 1x 330uF, 15x 22uF 0603, 25x 1uF 0402

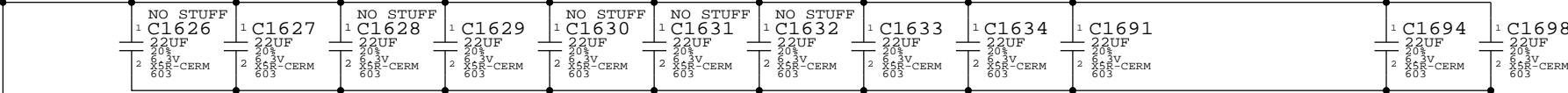
PLACEMENT_NOTE (C1600-C1624):

Place on bottom side of U1000..



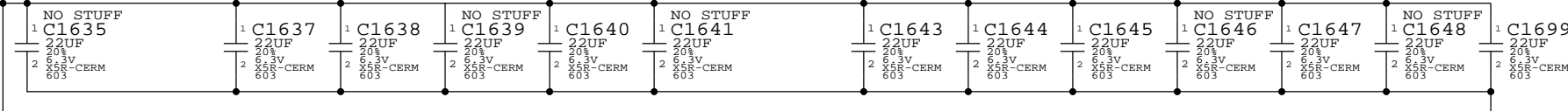
PLACEMENT_NOTE (C1625-C1634):

Place near U1000 on bottom side.



PLACEMENT_NOTE (C1635-C1648):

Place near inductors on bottom side.

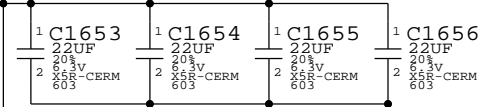


VTT (CPU Uncore) DECOUPLING

3x 330uF 6 mOhm, 4x 22uF 0805, 7x 10uF 0603, 24x 1uF 0402

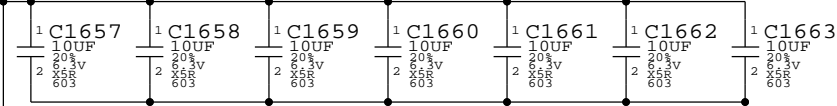
PLACEMENT_NOTE (C1653-C1656):

Place on bottom side of U1000..



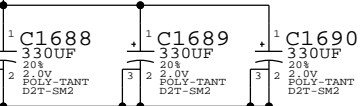
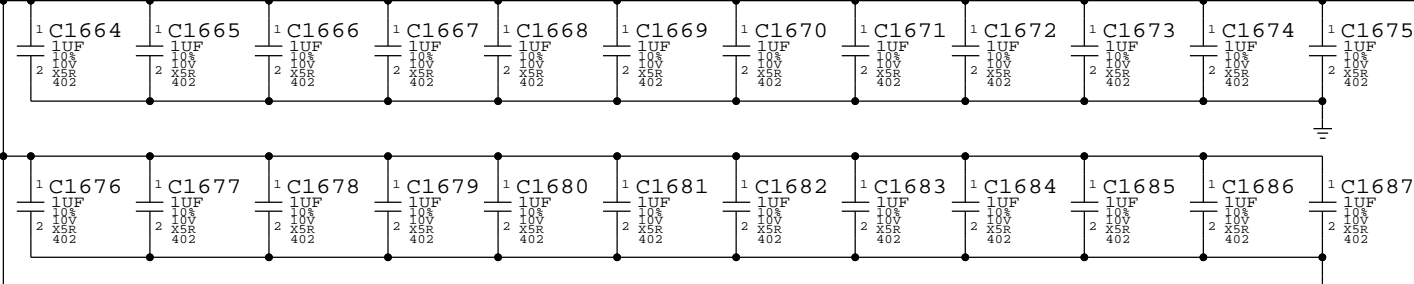
PLACEMENT_NOTE (C1657-C1663):

Place on bottom side of U1000..



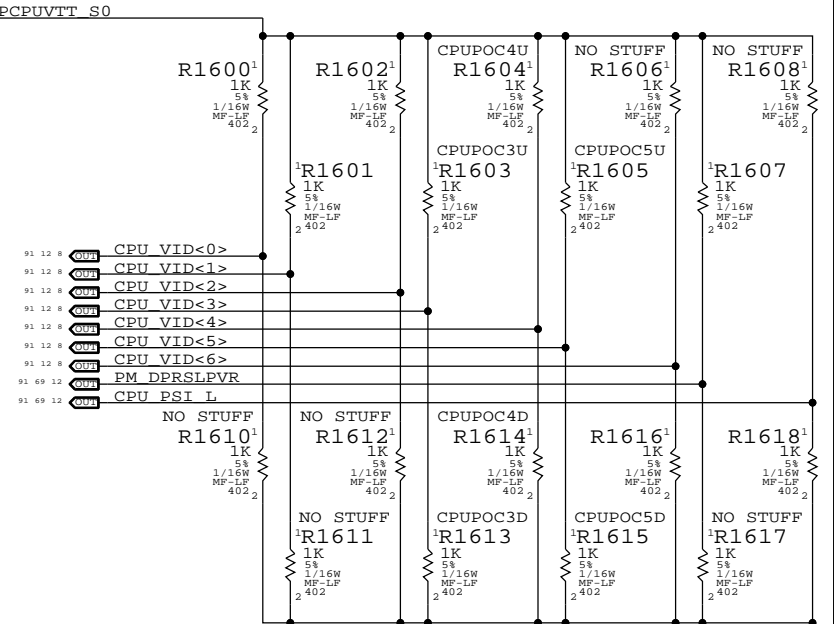
PLACEMENT_NOTE (C1664-C1687):

Place on bottom side of U1000.



CPU Power On Configuration (POC) Straps

Intel recommends all option straps should be provided in layout



VID[2:0] = Reserved (111)
VID[5:3] = GPU Gain Setting (See below)
VID[6] = Reserved (0)
DPRSLPVR = 1 - IMVP-6.5 compliant controller
PSI# = Reserved (0)

BOM GROUP	IMAX @ 900mV	CPU Gain Setting	BOM OPTIONS	Equivalent Gain
CPUPROC_IMAX_DIS		000	CPUPROC3D,CPUPROC4D,CPUPROC5D	
CPUPROC_IMAX_0_20	20A	001	CPUPROC3D,CPUPROC4D,CPUPROC5U	45
CPUPROC_IMAX_20_30	30A	010	CPUPROC3D,CPUPROC4U,CPUPROC5D	30
CPUPROC_IMAX_30_40	40A	011	CPUPROC3D,CPUPROC4U,CPUPROC5U	22.5
CPUPROC_IMAX_40_50	50A	100	CPUPROC3U,CPUPROC4D,CPUPROC5D	18
CPUPROC_IMAX_50_60	60A	101	CPUPROC3U,CPUPROC4D,CPUPROC5U	15
CPUPROC_IMAX_60_70	70A	110	CPUPROC3U,CPUPROC4U,CPUPROC5D	12.857
CPUPROC_IMAX_70_90	90A	111	CPUPROC3U,CPUPROC4U,CPUPROC5U	10

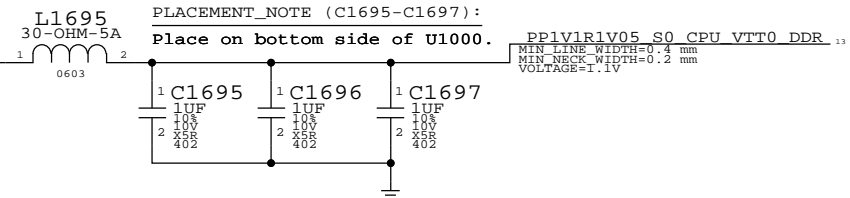
NOTE: BOM Configurations should not call out CPUPOCnU/D BOMOPTIONS directly.
Instead call out appropriate BOM GROUP defined in tables above.

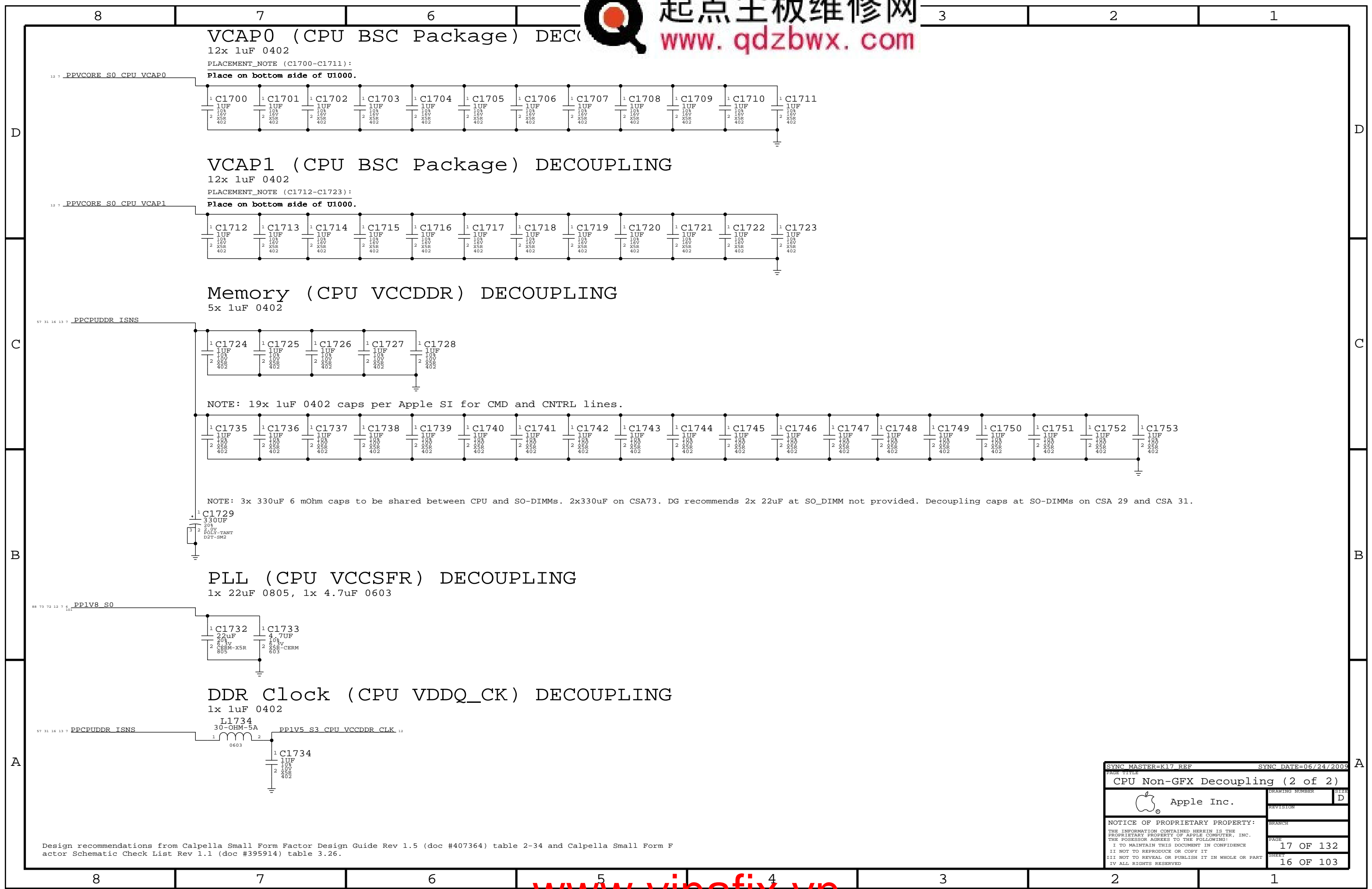
VTT0_DDR DECOUPLING

3x 1uF 0402

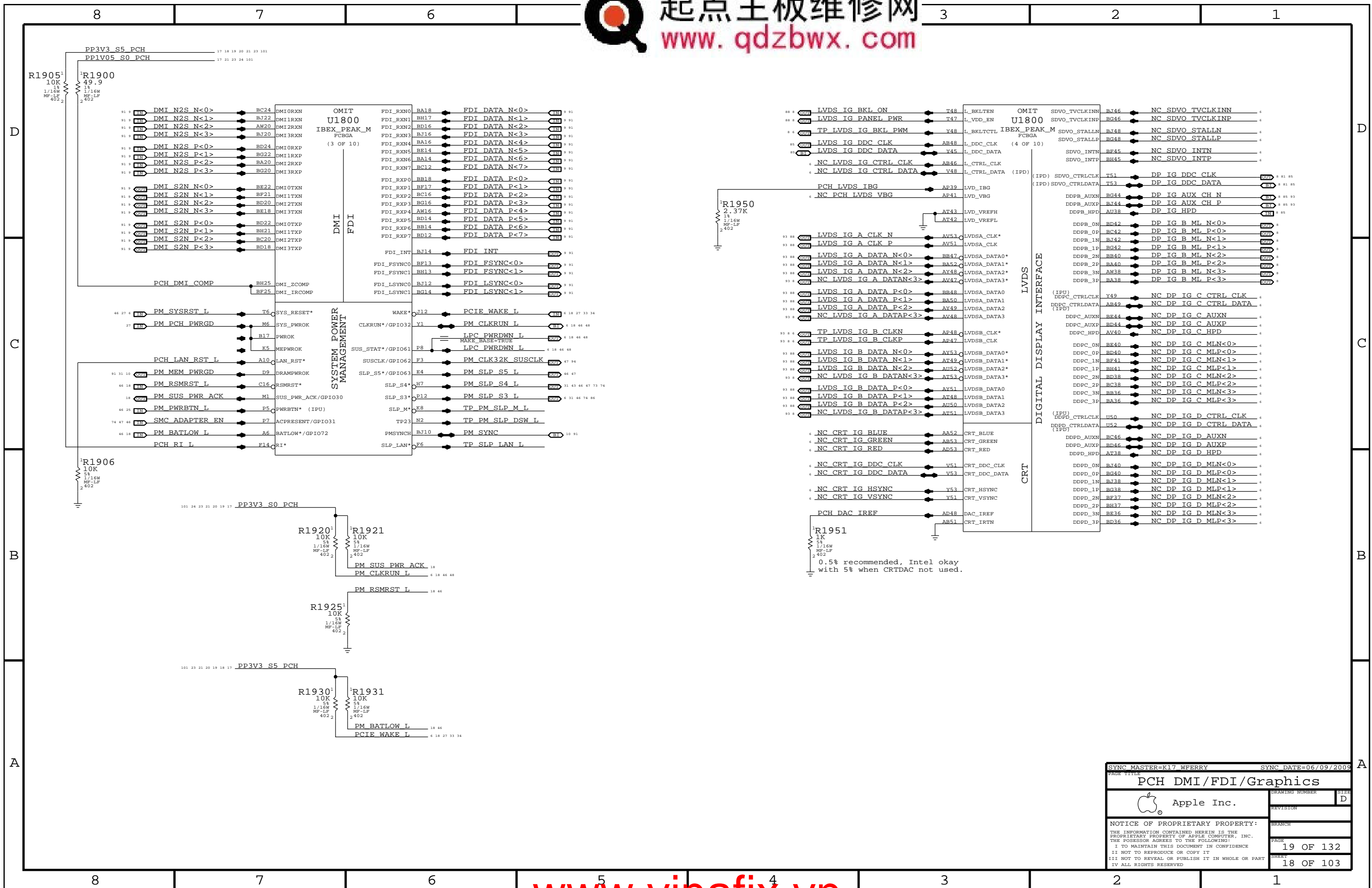
PLACEMENT_NOTE (C1695-C1697):

Place on bottom side of U1000.











D

C

B

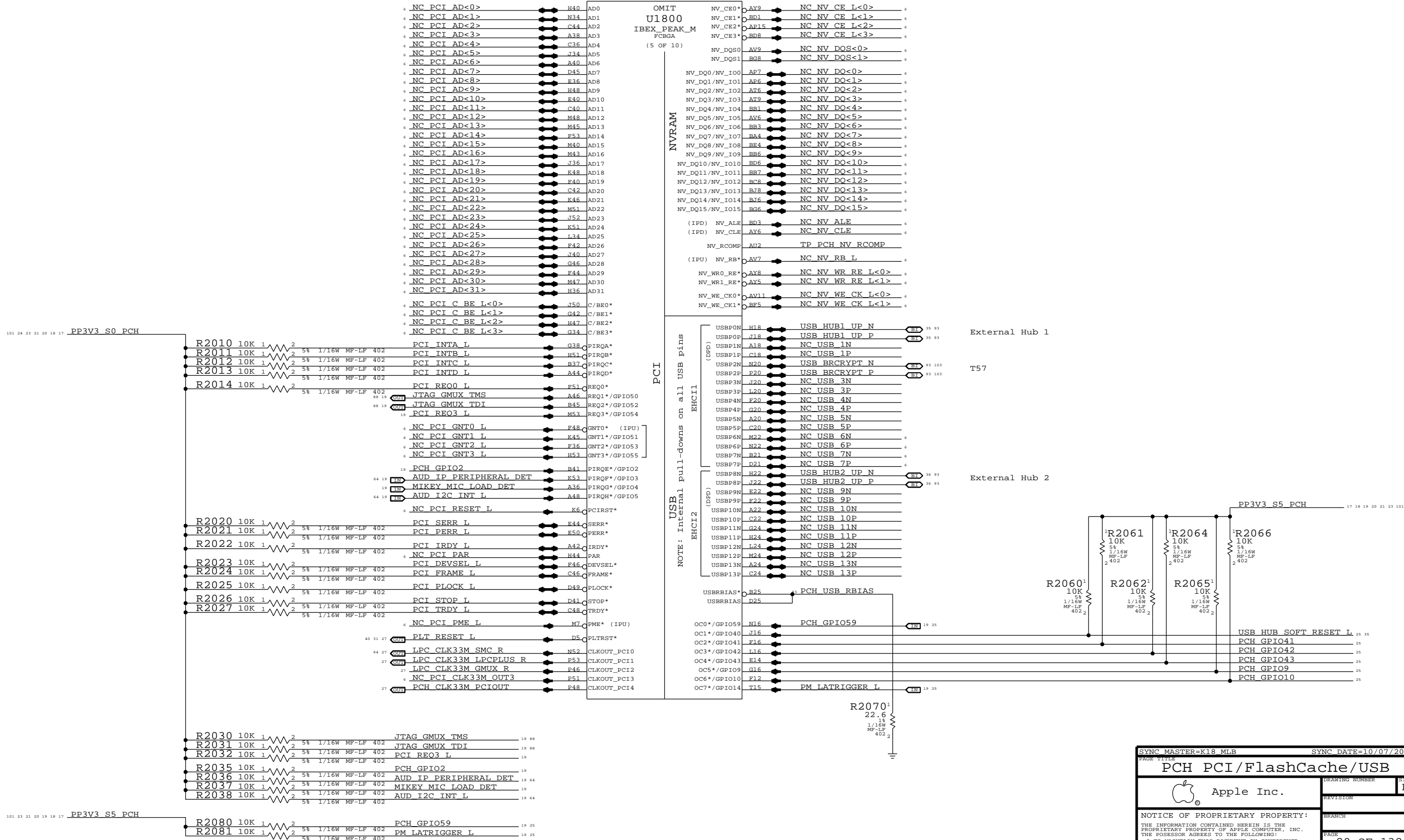
A

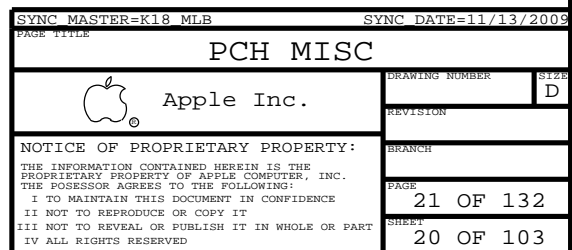
D

C

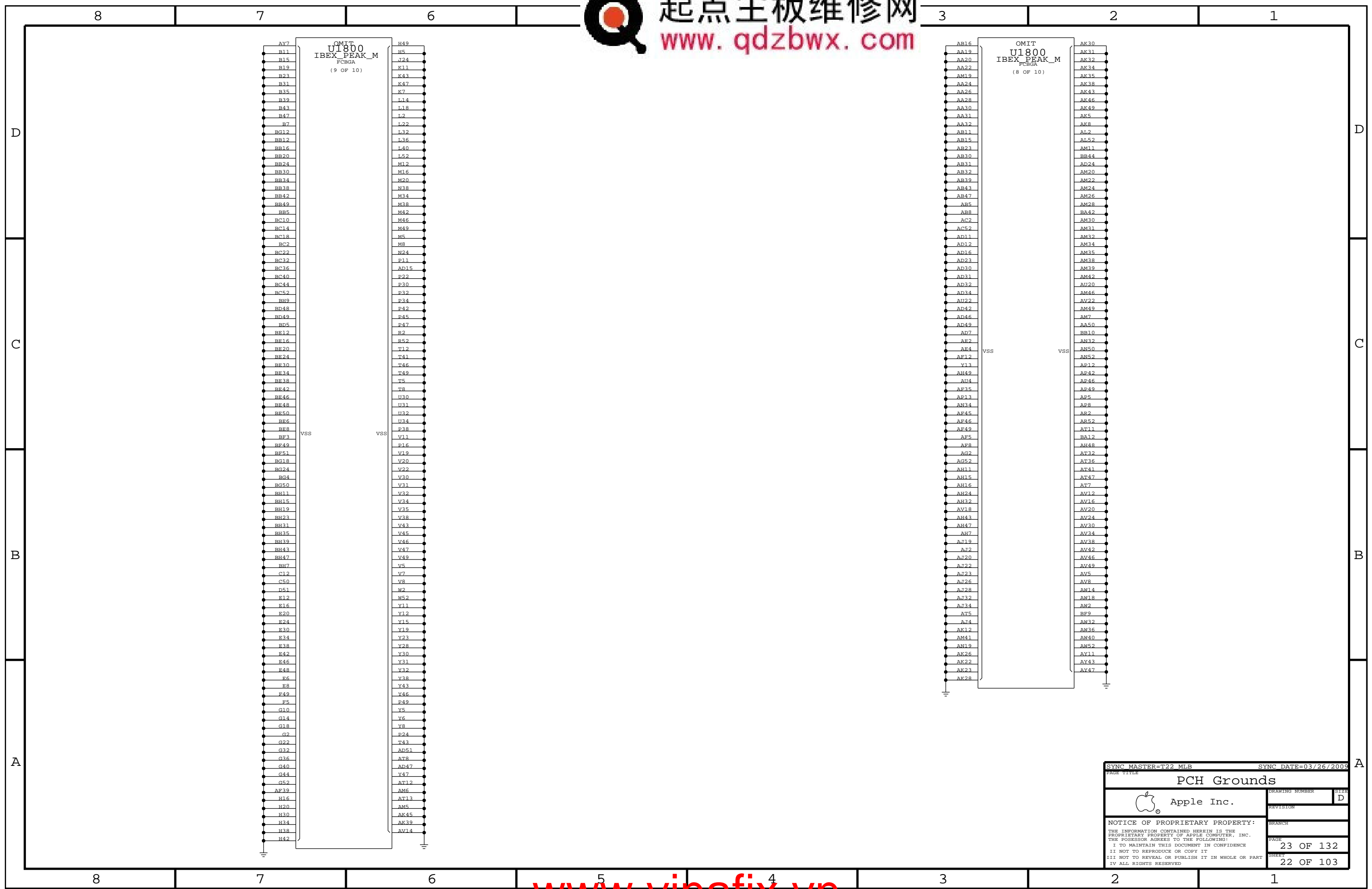
B

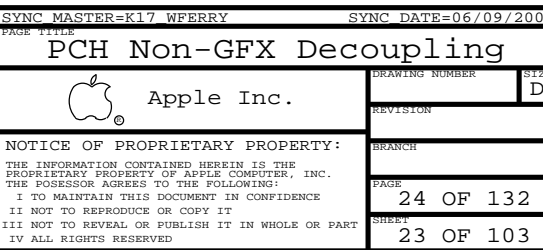
A











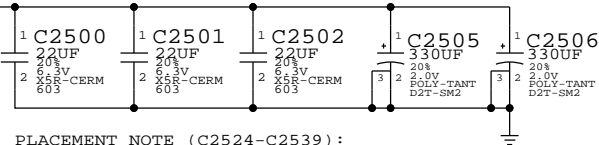


GFX (CPU VCCAXG) DECOUPLING

3x 330uF 6 mOhm (2 stuffed), 3x 22uF 0603,

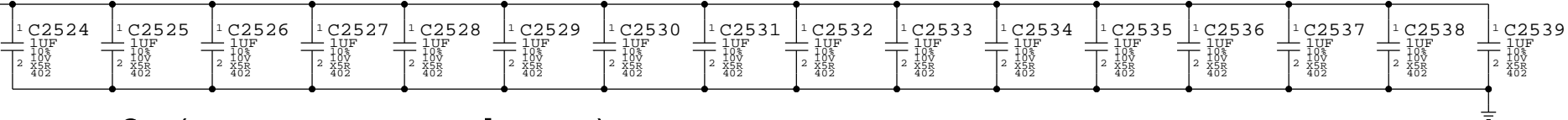
PLACEMENT_NOTE (C2500-C2506):

Place on bottom side of U1000.



PLACEMENT_NOTE (C2524-C2539):

Place on bottom side of U1000.

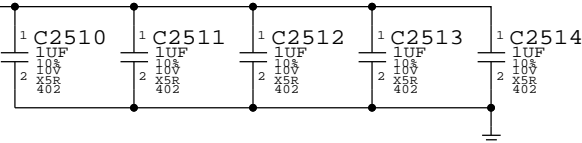


VCAP2 (CPU BSC Package) DECOUPLING

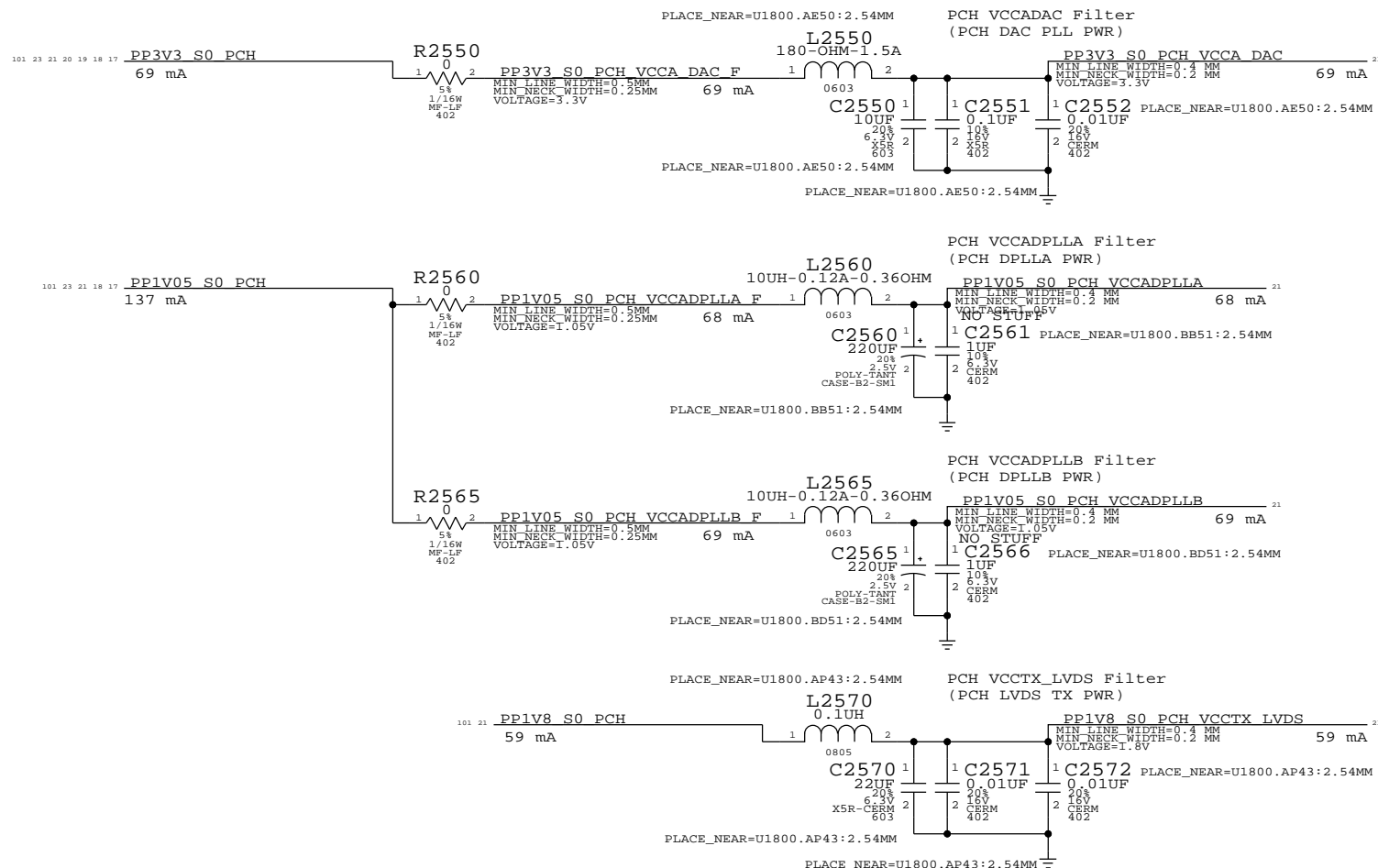
5x 1uF 0402

PLACEMENT_NOTE (C2510-C2514):

Place on bottom side of U1000.




Design recommendations from Calpella Small Form Factor Design Guide Rev 1.5 (doc #407364) table 2-34 and Calpella Small Form F actor Schematic Check List Rev 1.1 (doc #395914) table 3.26.



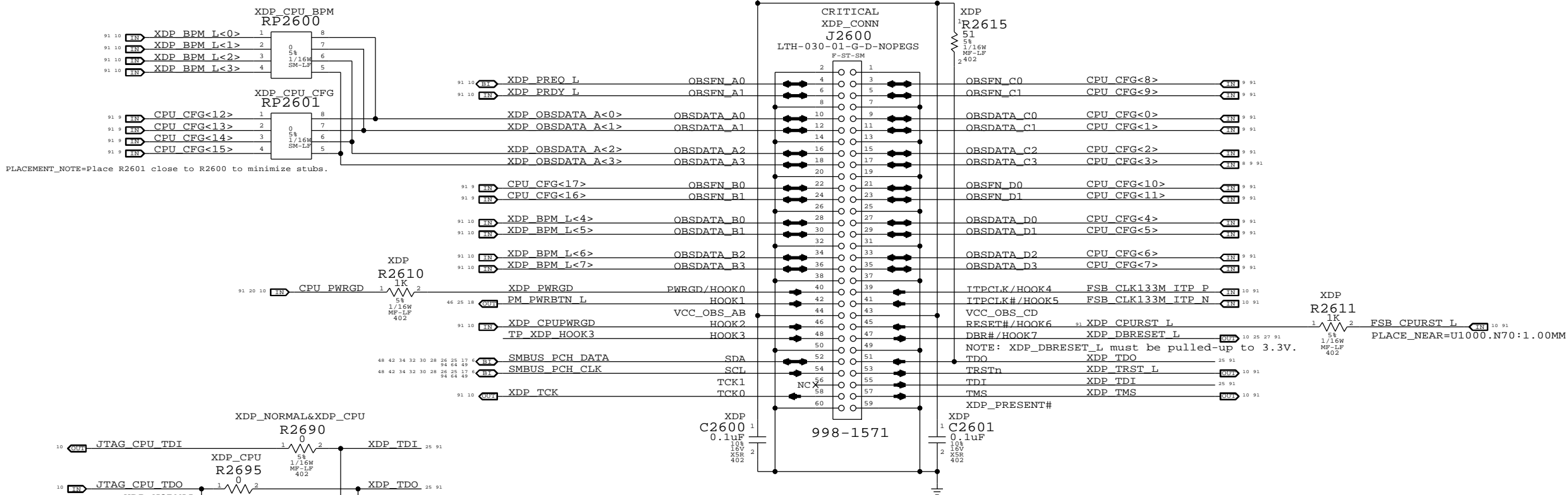
Design recommendations from Calpella Design Guide Rev 1.5 (doc #398905) Section 3.25.3 tables 161 and 162.

Current numbers from Ibox Peak EDS Spec Update rev 0.71, doc #386904 (Table 8-3). Pre-Silicon Mobile Estimates.

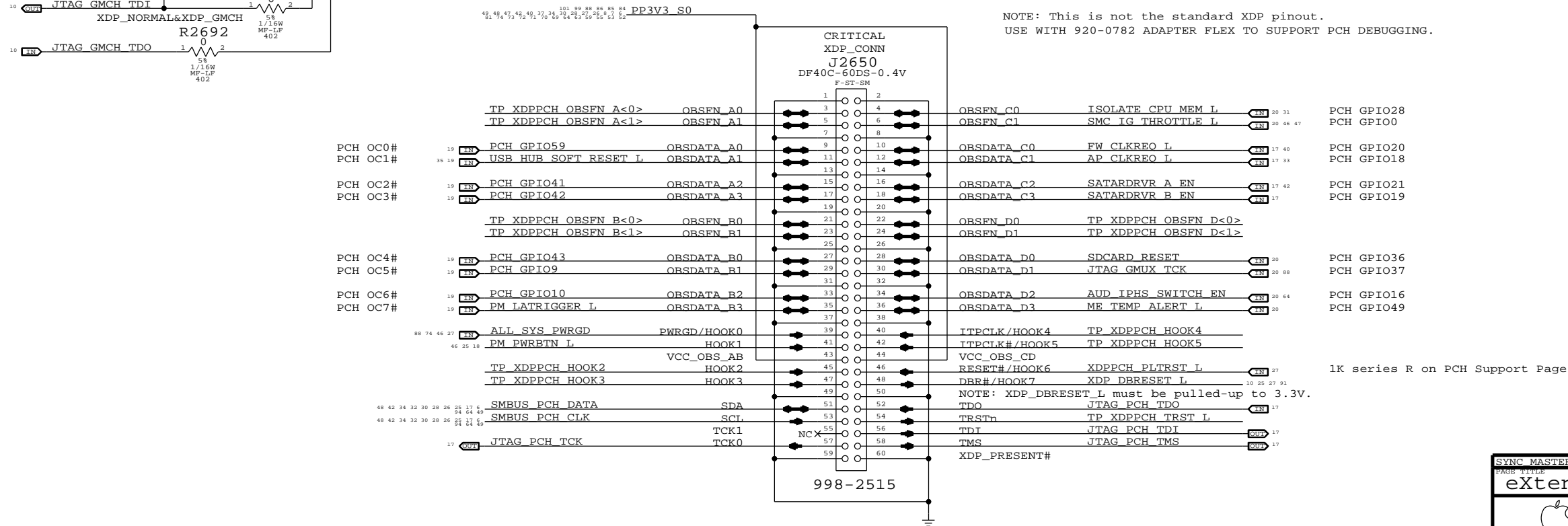
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CPU/PCH GFX Decoupling			
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		PAGE	25 OF 132
		SHEET	24 OF 103



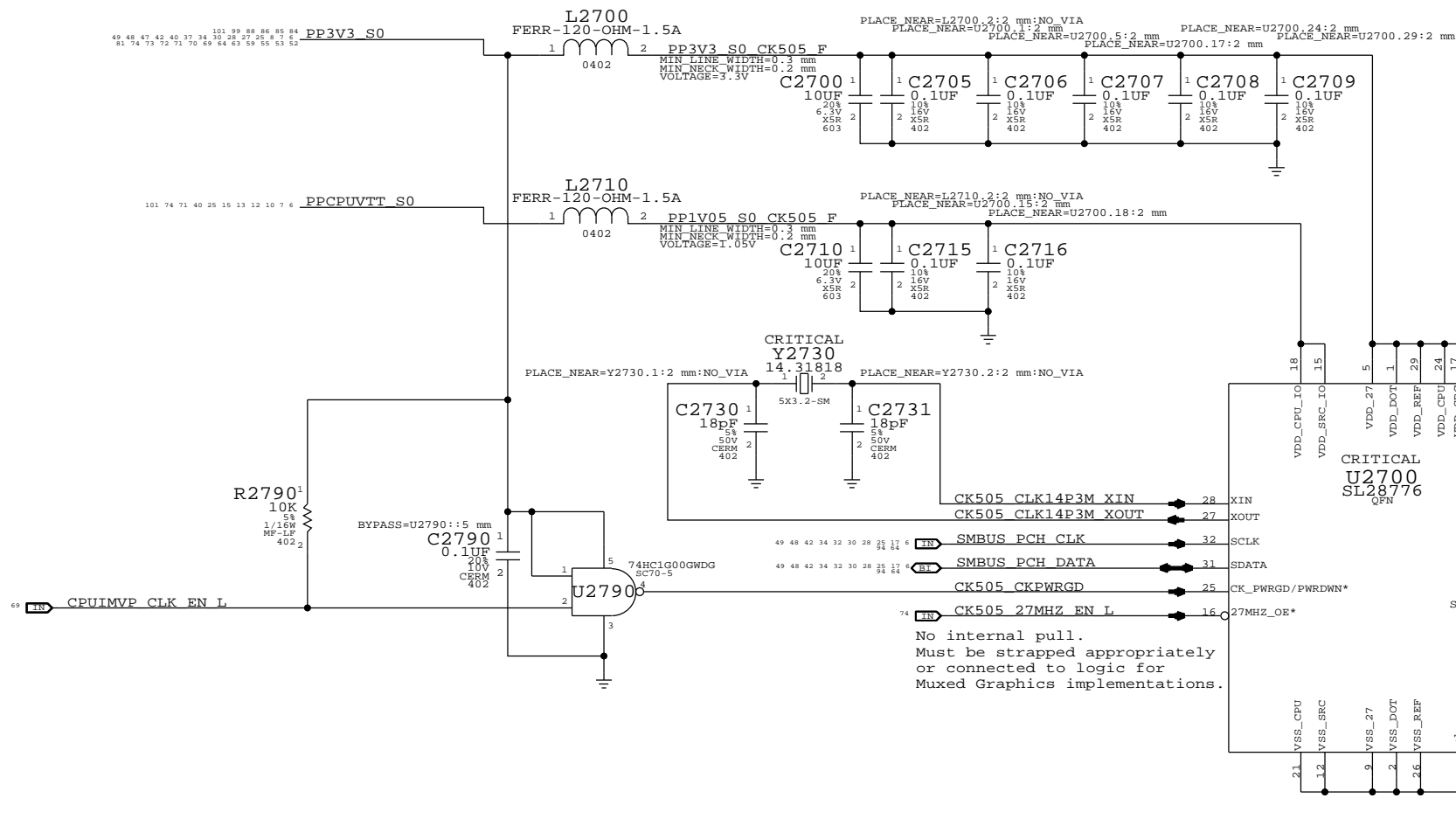
Calpel



Calpella PCH mini XDP



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eXtended Debug Port (XDP)			
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PAGE		SHEET	
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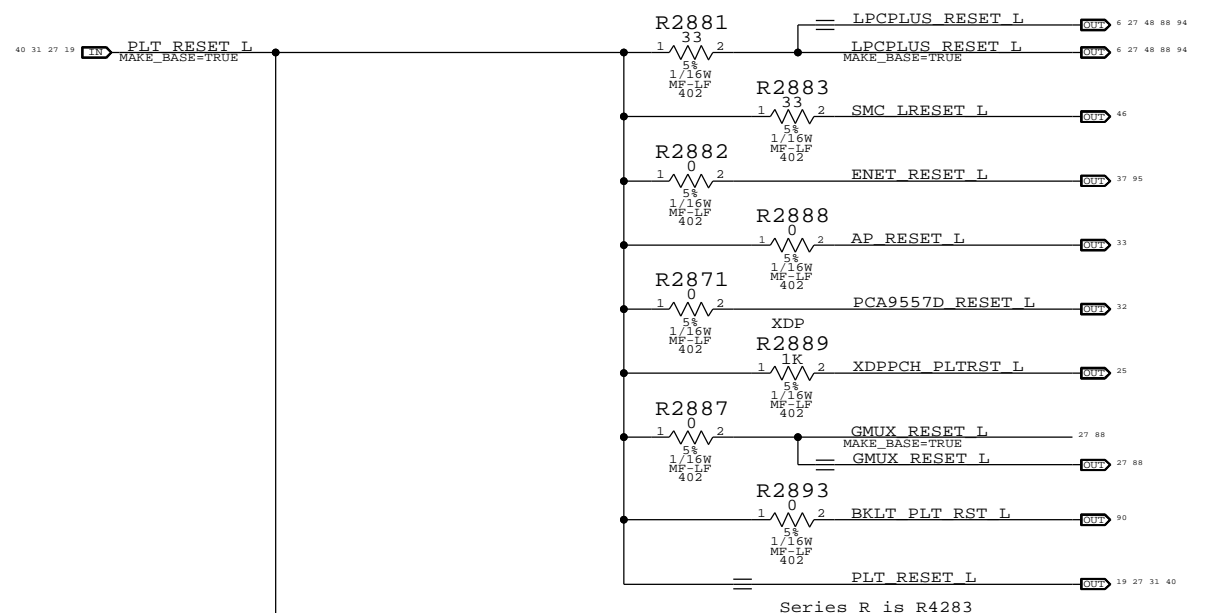


- NOTE: REF/FS pin is input until first CK_PWRGD rising edge.
FS=0 => 133MHz BCLKs, FS=1 => 100MHz BCLKs
All other output frequencies are fixed.
- | Pin | Signal | Frequency |
|-----|---------------------|---------------------------------|
| 30 | PCH CLK14P3M REFCLK | PCH REFCLK 14.31818MHz |
| 8 | TP CK505 USB | Unused 48MHz |
| 22 | FSB CLK133M PCH N | PCH BCLK 133MHz |
| 23 | FSB CLK133M PCH P | Unused BCLK 133MHz |
| 19 | TP CK505 CPU1N | PCH DMI/PCIe 100MHz |
| 20 | TP CK505 CPU1P | PCH SATA 100MHz |
| 14 | PCIE CLK100M PCH N | GPU 27MHz Clocks (Single-Ended) |
| 13 | PCIE CLK100M PCH P | PCH USB Clock 96MHz |
| 11 | PCH CLK100M SATA N | |
| 10 | PCH CLK100M SATA P | |
| 6 | CK505 CLK27M | |
| 7 | TP CK505 CLK27M SS | |
| 4 | PCH CLK96M DOT N | |
| 3 | PCH CLK96M DOT P | |

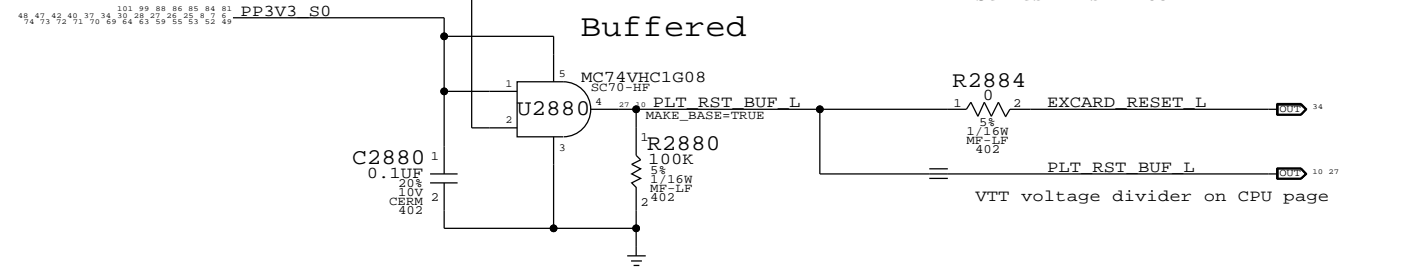


Platform Reset Connections

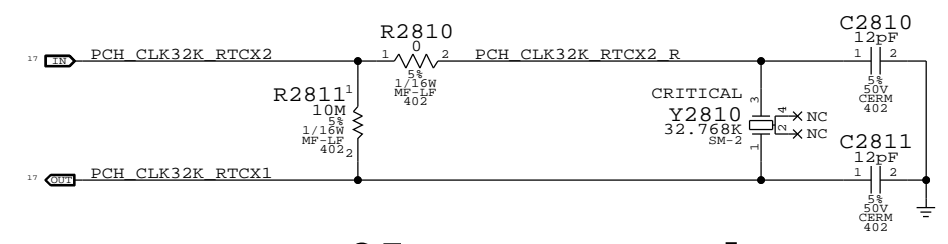
Unbuffered



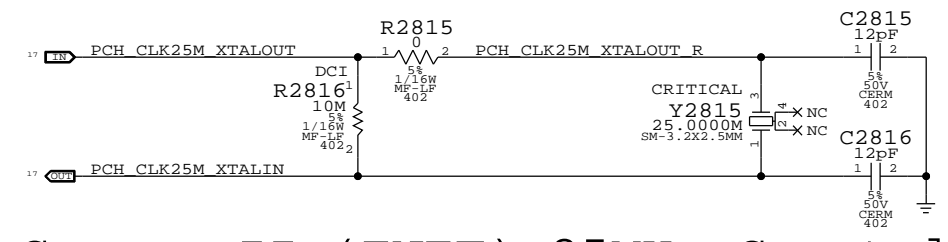
Buffered



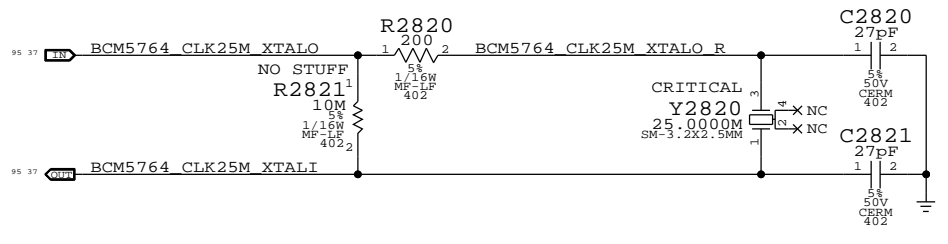
PCH RTC Crystal



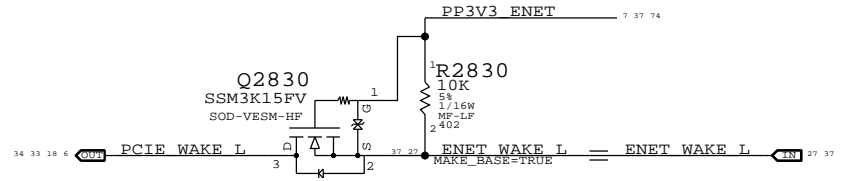
PCH 25MHz Crystal



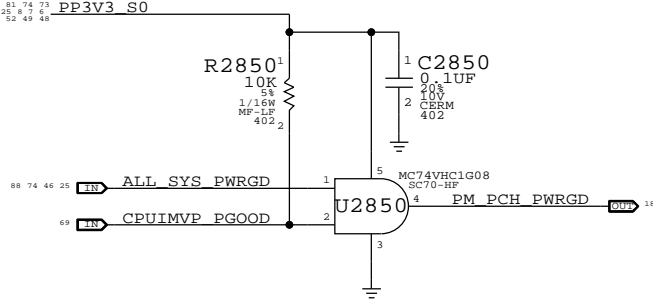
Caesar II (ENET) 25MHz Crystal



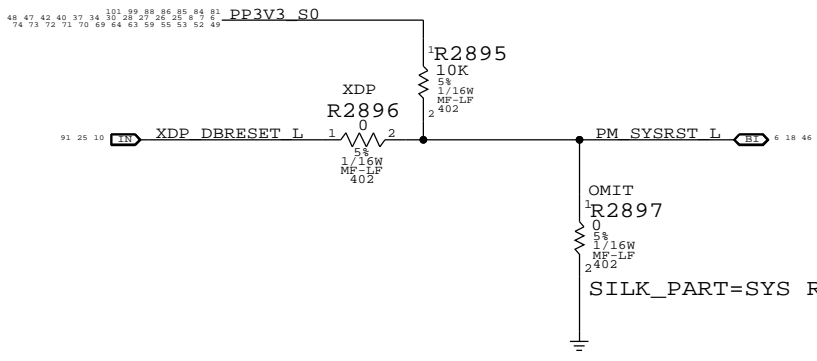
Ethernet WAKE# Isolation



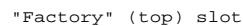
PCH S0 PWRGD



PCH Reset Button



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Chipset Support		DRAWING NUMBER	SIZE
Apple Inc.		REVISION	D
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8				7				6				3				2				1											
CPU CHANNEL A DQS 0 -> DIMM A DQS 0																CPU CHANNEL B DQS 0 -> DIMM B DQS 0															
MEM A DQS N<0> MAKE_BASE=TRUE == MEM A DQS N<0>																MEM B DQS N<0> MAKE_BASE=TRUE == MEM B DQS N<0>															
MEM A DQS P<0> MAKE_BASE=TRUE == MEM A DQS P<0>																MEM B DQS P<0> MAKE_BASE=TRUE == MEM B DQS P<0>															
MEM A DM<0> MAKE_BASE=TRUE == MEM A DM<0>																MEM B DM<0> MAKE_BASE=TRUE == MEM B DM<0>															
MEM A DQ<7> MAKE_BASE=TRUE == MEM A DQ<7>																MEM B DQ<7> MAKE_BASE=TRUE == MEM B DQ<7>															
MEM A DQ<6> MAKE_BASE=TRUE == MEM A DQ<6>																MEM B DQ<6> MAKE_BASE=TRUE == MEM B DQ<6>															
MEM A DQ<5> MAKE_BASE=TRUE == MEM A DQ<5>																MEM B DQ<5> MAKE_BASE=TRUE == MEM B DQ<5>															
MEM A DQ<4> MAKE_BASE=TRUE == MEM A DQ<4>																MEM B DQ<4> MAKE_BASE=TRUE == MEM B DQ<4>															
MEM A DQ<3> MAKE_BASE=TRUE == MEM A DQ<3>																MEM B DQ<3> MAKE_BASE=TRUE == MEM B DQ<3>															
MEM A DQ<2> MAKE_BASE=TRUE == MEM A DQ<2>																MEM B DQ<2> MAKE_BASE=TRUE == MEM B DQ<2>															
MEM A DQ<1> MAKE_BASE=TRUE == MEM A DQ<1>																MEM B DQ<1> MAKE_BASE=TRUE == MEM B DQ<1>															
MEM A DQ<0> MAKE_BASE=TRUE == MEM A DQ<0>																MEM B DQ<0> MAKE_BASE=TRUE == MEM B DQ<0>															
CPU CHANNEL A DQS 1 -> DIMM A DQS 1																CPU CHANNEL B DQS 1 -> DIMM B DQS 1															
MEM A DQS N<1> MAKE_BASE=TRUE == MEM A DQS N<1>																MEM B DQS N<1> MAKE_BASE=TRUE == MEM B DQS N<1>															
MEM A DQS P<1> MAKE_BASE=TRUE == MEM A DQS P<1>																MEM B DQS P<1> MAKE_BASE=TRUE == MEM B DQS P<1>															
MEM A DM<1> MAKE_BASE=TRUE == MEM A DM<1>																MEM B DM<1> MAKE_BASE=TRUE == MEM B DM<1>															
MEM A DQ<15> MAKE_BASE=TRUE == MEM A DQ<15>																MEM B DQ<15> MAKE_BASE=TRUE == MEM B DQ<15>															
MEM A DQ<14> MAKE_BASE=TRUE == MEM A DQ<14>																MEM B DQ<14> MAKE_BASE=TRUE == MEM B DQ<14>															
MEM A DQ<13> MAKE_BASE=TRUE == MEM A DQ<13>																MEM B DQ<13> MAKE_BASE=TRUE == MEM B DQ<13>															
MEM A DQ<12> MAKE_BASE=TRUE == MEM A DQ<12>																MEM B DQ<12> MAKE_BASE=TRUE == MEM B DQ<12>															
MEM A DQ<11> MAKE_BASE=TRUE == MEM A DQ<11>																MEM B DQ<11> MAKE_BASE=TRUE == MEM B DQ<11>															
MEM A DQ<10> MAKE_BASE=TRUE == MEM A DQ<10>																MEM B DQ<10> MAKE_BASE=TRUE == MEM B DQ<10>															
MEM A DQ<9> MAKE_BASE=TRUE == MEM A DQ<9>																MEM B DQ<9> MAKE_BASE=TRUE == MEM B DQ<9>															
MEM A DQ<8> MAKE_BASE=TRUE == MEM A DQ<8>																MEM B DQ<8> MAKE_BASE=TRUE == MEM B DQ<8>															
CPU CHANNEL A DQS 2 -> DIMM A DQS 2																CPU CHANNEL B DQS 2 -> DIMM B DQS 2															
MEM A DQS N<2> MAKE_BASE=TRUE == MEM A DQS N<2>																MEM B DQS N<2> MAKE_BASE=TRUE == MEM B DQS N<2>															
MEM A DQS P<2> MAKE_BASE=TRUE == MEM A DQS P<2>																MEM B DQS P<2> MAKE_BASE=TRUE == MEM B DQS P<2>															
MEM A DM<2> MAKE_BASE=TRUE == MEM A DM<2>																MEM B DM<2> MAKE_BASE=TRUE == MEM B DM<2>															
MEM A DQ<23> MAKE_BASE=TRUE == MEM A DQ<23>																MEM B DQ<23> MAKE_BASE=TRUE == MEM B DQ<23>															
MEM A DQ<22> MAKE_BASE=TRUE == MEM A DQ<22>																MEM B DQ<22> MAKE_BASE=TRUE == MEM B DQ<22>															
MEM A DQ<21> MAKE_BASE=TRUE == MEM A DQ<21>																MEM B DQ<21> MAKE_BASE=TRUE == MEM B DQ<21>															
MEM A DQ<20> MAKE_BASE=TRUE == MEM A DQ<20>																MEM B DQ<20> MAKE_BASE=TRUE == MEM B DQ<20>															
MEM A DQ<19> MAKE_BASE=TRUE == MEM A DQ<19>																MEM B DQ<19> MAKE_BASE=TRUE == MEM B DQ<19>															
MEM A DQ<18> MAKE_BASE=TRUE == MEM A DQ<18>																MEM B DQ<18> MAKE_BASE=TRUE == MEM B DQ<18>															
MEM A DQ<17> MAKE_BASE=TRUE == MEM A DQ<17>																MEM B DQ<17> MAKE_BASE=TRUE == MEM B DQ<17>															
MEM A DQ<16> MAKE_BASE=TRUE == MEM A DQ<16>																MEM B DQ<16> MAKE_BASE=TRUE == MEM B DQ<16>															
CPU CHANNEL A DQS 3 -> DIMM A DQS 3																CPU CHANNEL B DQS 3 -> DIMM B DQS 3															
MEM A DQS N<3> MAKE_BASE=TRUE == MEM A DQS N<3>																MEM B DQS N<3> MAKE_BASE=TRUE == MEM B DQS N<3>															
MEM A DQS P<3> MAKE_BASE=TRUE == MEM A DQS P<3>																MEM B DQS P<3> MAKE_BASE=TRUE == MEM B DQS P<3>															
MEM A DM<3> MAKE_BASE=TRUE == MEM A DM<3>																MEM B DM<3> MAKE_BASE=TRUE == MEM B DM<3>															
MEM A DQ<31> MAKE_BASE=TRUE == MEM A DQ<31>																MEM B DQ<31> MAKE_BASE=TRUE == MEM B DQ<31>															
MEM A DQ<30> MAKE_BASE=TRUE == MEM A DQ<30>																MEM B DQ<30> MAKE_BASE=TRUE == MEM B DQ<30>															
MEM A DQ<29> MAKE_BASE=TRUE == MEM A DQ<29>																MEM B DQ<29> MAKE_BASE=TRUE == MEM B DQ<29>															
MEM A DQ<28> MAKE_BASE=TRUE == MEM A DQ<28>																MEM B DQ<28> MAKE_BASE=TRUE == MEM B DQ<28>															
MEM A DQ<27> MAKE_BASE=TRUE == MEM A DQ<27>																MEM B DQ<27> MAKE_BASE=TRUE == MEM B DQ<27>															
MEM A DQ<26> MAKE_BASE=TRUE == MEM A DQ<26>																MEM B DQ<26> MAKE_BASE=TRUE == MEM B DQ<26>															
MEM A DQ<25> MAKE_BASE=TRUE == MEM A DQ<25>																MEM B DQ<25> MAKE_BASE=TRUE == MEM B DQ<25>															
MEM A DQ<24> MAKE_BASE=TRUE == MEM A DQ<24>																MEM B DQ<24> MAKE_BASE=TRUE == MEM B DQ<24>															
CPU CHANNEL A DQS 4 -> DIMM A DQS 4																CPU CHANNEL B DQS 4 -> DIMM B DQS 4															
MEM A DQS N<4> MAKE_BASE=TRUE == MEM A DQS N<4>																MEM B DQS N<4> MAKE_BASE=TRUE == MEM B DQS N<4>															
MEM A DQS P<4> MAKE_BASE=TRUE == MEM A DQS P<4>																MEM B DQS P<4> MAKE_BASE=TRUE == MEM B DQS P<4>															
MEM A DM<4> MAKE_BASE=TRUE == MEM A DM<4>																MEM B DM<4> MAKE_BASE=TRUE == MEM B DM<4>															
MEM A DQ<39> MAKE_BASE=TRUE == MEM A DQ<39>																MEM B DQ<39> MAKE_BASE=TRUE == MEM B DQ<39>															
MEM A DQ<38> MAKE_BASE=TRUE == MEM A DQ<38>																MEM B DQ<38> MAKE_BASE=TRUE == MEM B DQ<38>															
MEM A DQ<37> MAKE_BASE=TRUE == MEM A DQ<37>																MEM B DQ<37> MAKE_BASE=TRUE == MEM B DQ<37>															
MEM A DQ<36> MAKE_BASE=TRUE == MEM A DQ<36>																MEM B DQ<36> MAKE_BASE=TRUE == MEM B DQ<36>															
MEM A DQ<35> MAKE_BASE=TRUE == MEM A DQ<35>																MEM B DQ<35> MAKE_BASE=TRUE == MEM B DQ<35>															
MEM A DQ<34> MAKE_BASE=TRUE == MEM A DQ<34>																MEM B DQ<34> MAKE_BASE=TRUE == MEM B DQ<34>															
MEM A DQ<33> MAKE_BASE=TRUE == MEM A DQ<33>																MEM B DQ<33> MAKE_BASE=TRUE == MEM B DQ<33>															
MEM A DQ<32> MAKE_BASE=TRUE == MEM A DQ<32>																MEM B DQ<32> MAKE_BASE=TRUE == MEM B DQ<32>															
CPU CHANNEL A DQS 5 -> DIMM A DQS 5																CPU CHANNEL B DQS 5 -> DIMM B DQS 5															
MEM A DQS N<5> MAKE_BASE=TRUE == MEM A DQS N<5>																MEM B DQS N<5> MAKE_BASE=TRUE == MEM B DQS N<5>															
MEM A DQS P<5> MAKE_BASE=TRUE == MEM A DQS P<5>																MEM B DQS P<5> MAKE_BASE=TRUE == MEM B DQS P<5>															
MEM A DM<5> MAKE_BASE=TRUE == MEM A DM<5>																MEM B DM<5> MAKE_BASE=TRUE == MEM B DM<5>															
MEM A DQ<47> MAKE_BASE=TRUE == MEM A DQ<47>																MEM B DQ<47> MAKE_BASE=TRUE == MEM B DQ<47>															
MEM A DQ<46> MAKE_BASE=TRUE == MEM A DQ<46>																MEM B DQ<46> MAKE_BASE=TRUE == MEM B DQ<46>															
MEM A DQ<45> MAKE_BASE=TRUE == MEM A DQ<45>																MEM B DQ<45> MAKE_BASE=TRUE == MEM B DQ<45>															
MEM A DQ<44> MAKE_BASE=TRUE == MEM A DQ<44>																MEM B DQ<44> MAKE_BASE=TRUE == MEM B DQ<44>															
MEM A DQ<43> MAKE_BASE=TRUE == MEM A DQ<43>																MEM B DQ<43> MAKE_BASE=TRUE == MEM B DQ<43>															
MEM A DQ<42> MAKE_BASE=TRUE == MEM A DQ<42>																MEM B DQ<42> MAKE_BASE=TRUE == MEM B DQ<42>															
MEM A DQ<41> MAKE_BASE=TRUE == MEM A DQ<41>																MEM B DQ<41> MAKE_BASE=TRUE == MEM B DQ<41>															
MEM A DQ<40> MAKE_BASE=TRUE == MEM A DQ<40>																MEM B DQ<40> MAKE_BASE=TRUE == MEM B DQ<40>															
CPU CHANNEL A DQS 6 -> DIMM A DQS 6																CPU CHANNEL B DQS 6 -> DIMM B DQS 6															
MEM A DQS N<6> MAKE_BASE=TRUE == MEM A DQS N<6>																MEM B DQS N<6> MAKE_BASE=TRUE == MEM B DQS N<6>															
MEM A DQS P<6> MAKE_BASE=TRUE == MEM A DQS P<6>																MEM B DQS P<6> MAKE_BASE=TRUE == MEM B DQS P<6>															
MEM A DM<6> MAKE_BASE=TRUE == MEM A DM<6>																MEM B DM<6> MAKE_BASE=TRUE == MEM B DM<6>															
MEM A DQ<55> MAKE_BASE=TRUE == MEM A DQ<55>																MEM B DQ<55> MAKE_BASE=TRUE == MEM B DQ<55>															
MEM A DQ<54> MAKE_BASE=TRUE == MEM A DQ<54>																MEM B DQ<54> MAKE_BASE=TRUE == MEM B DQ<54>															
MEM A DQ<53> MAKE_BASE=TRUE == MEM A DQ<53>																MEM B DQ<53> MAKE_BASE=TRUE == MEM B DQ<53>															
MEM A DQ<52> MAKE_BASE=TRUE == MEM A DQ<52>																MEM B DQ<52> MAKE_BASE=TRUE == MEM B DQ<52>															
MEM A DQ<51> MAKE_BASE=TRUE == MEM A DQ<51>																MEM B DQ<51> MAKE_BASE=TRUE == MEM B DQ<51>															
MEM A DQ<50> MAKE_BASE=TRUE == MEM A DQ<50>																MEM B DQ<50> MAKE_BASE=TRUE == MEM B DQ<50>															
MEM A DQ<49> MAKE_BASE=TRUE == MEM A DQ<49>																MEM B DQ<49> MAKE_BASE=TRUE == MEM B DQ<49>															
MEM A DQ<48> MAKE_BASE=TRUE == MEM A DQ<48>																MEM B DQ<48> MAKE_BASE=TRUE == MEM B DQ<48>															
CPU CHANNEL A DQS 7 -> DIMM A DQS 7																CPU CHANNEL B DQS 7 -> DIMM B DQS 7															
MEM A DQS N<7> MAKE_BASE=TRUE == MEM A DQS N<7>																MEM B DQS N<7> MAKE_BASE=TRUE == MEM B DQS N<7>															
MEM A DQS P<7> MAKE_BASE=TRUE == MEM A DQS P<7>																MEM B DQS P<7> MAKE_BASE=TRUE == MEM B DQS P<7>															
MEM A DM<7> MAKE_BASE=TRUE == MEM A DM<7>																MEM B DM<7> MAKE_BASE=TRUE == MEM B DM<7>															
MEM A DQ<63> MAKE_BASE=TRUE == MEM A DQ<63>																MEM B DQ<63> MAKE_BASE=TRUE == MEM B DQ<63>															
MEM A DQ<62> MAKE_BASE=TRUE == MEM A DQ<62>																MEM B DQ<62> MAKE_BASE=TRUE == MEM B DQ<62>															
MEM A DQ<61> MAKE_BASE=TRUE == MEM A DQ<61>																MEM B DQ<61> MAKE_BASE=TRUE == MEM B DQ<61>															
MEM A DQ<60> MAKE_BASE=TRUE == MEM A DQ<60>																MEM B DQ<60> MAKE_BASE=TRUE == MEM B DQ<60>															
MEM A DQ<59> MAKE_BASE=TRUE == MEM A DQ<59>																MEM B DQ<59> MAKE_BASE=TRUE == MEM B DQ<59>															
MEM A DQ<58> MAKE_BASE=TRUE == MEM A DQ<58>																MEM B DQ<58> MAKE_BASE=TRUE == MEM B DQ<58>															
MEM A DQ<57> MAKE_BASE=TRUE == MEM A DQ<57>																MEM B DQ<57> MAKE_BASE=TRUE == MEM B DQ<57>															
MEM A DQ<56> MAKE_BASE=TRUE == MEM A DQ<56>																MEM B DQ<56> MAKE_BASE=TRUE == MEM B DQ<56>															
CPU CHANNEL A DQS 8 -> DIMM A DQS 8																CPU CHANNEL B DQS 8 -> DIMM B DQS 8															
MEM A DQS N<8> MAKE_BASE=TRUE == MEM A DQS N<8>																MEM B DQS N<8> MAKE_BASE=TRUE == MEM B DQS N<8>															
MEM A DQS P<8> MAKE_BASE=TRUE == MEM A DQS P<8>																MEM B DQS P<8> MAKE_BASE=TRUE == MEM B DQS P<8>															
MEM A DM<8> MAKE_BASE=TRUE == MEM A DM<8>																MEM B DM<8> MAKE_BASE=TRUE == MEM B DM<8>															
MEM A DQ<71> MAKE_BASE=TRUE == MEM A DQ<71>																MEM B DQ<71> MAKE_BASE=TRUE == MEM B DQ<71>															
MEM A DQ<70> MAKE_BASE=TRUE == MEM A DQ<70>																MEM B DQ<70> MAKE_BASE=TRUE == MEM B DQ<70>															
MEM A DQ<69> MAKE_BASE=TRUE == MEM A DQ<69>																MEM B DQ<69> MAKE_BASE=TRUE == MEM B DQ<69>															
MEM A DQ<68> MAKE_BASE=TRUE == MEM A DQ<68>																MEM B DQ<68> MAKE_BASE=TRUE == MEM B DQ<68>															
MEM A DQ<67> MAKE_BASE=TRUE == MEM A DQ<67>																MEM B DQ<67> MAKE_BASE=TRUE == MEM B DQ<67>															
MEM A DQ<66> MAKE_BASE=TRUE == MEM A DQ<66>																MEM B DQ<66> MAKE_BASE=TRUE == MEM B DQ<66>															
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MEM A DQ<64> MAKE_BASE=TRUE == MEM A DQ<64>																MEM B DQ<64> MAKE_BASE=TRUE == MEM B DQ<64>															
MEM A DQ<63> MAKE_BASE=TRUE == MEM A DQ<63>																MEM B DQ<63> MAKE_BASE=TRUE == MEM B DQ<63>															
MEM A DQ<62> MAKE_BASE=TRUE == MEM A DQ<62>																MEM B DQ<62> MAKE_BASE=TRUE == MEM B DQ<62>															
MEM A DQ<61> MAKE_BASE=TRUE == MEM A DQ<61>																MEM B DQ<61> MAKE_BASE=TRUE == MEM B DQ<61>															
MEM A DQ<60> MAKE_BASE=TRUE == MEM A DQ<60>																MEM B DQ<60> MAKE_BASE=TRUE == MEM B DQ<60>															
MEM A DQ<59> MAKE_BASE=TRUE == MEM A DQ<59>																MEM B DQ<59> MAKE_BASE=TRUE == MEM B DQ<59>															
MEM A DQ<58> MAKE_BASE=TRUE == MEM A DQ<58>																MEM B DQ<58> MAKE_BASE=TRUE == MEM B DQ<58>															
MEM A DQ<57> MAKE_BASE=TRUE == MEM A DQ<57>																MEM B DQ<57> MAKE_BASE=TRUE == MEM B DQ<57>															
MEM A DQ<56> MAKE_BASE=TRUE == MEM A DQ<56>																MEM B DQ<56> MAKE_BASE=TRUE == MEM B DQ<56>															
CPU CHANNEL A DQS 9 -> DIMM A DQS 9																CPU CHANNEL B DQS 9 -> DIMM B DQS 9															
MEM A DQS N<9> MAKE_BASE=TRUE == MEM A DQS N<9>																MEM B DQS N<9> MAKE_BASE=TRUE == MEM B DQS N<9>															
MEM A DQS P<9> MAKE_BASE=TRUE == MEM A DQS P<9>																MEM B DQS P<9> MAKE_BASE=TRUE == MEM B DQS P<9>															
MEM A DM<9> MAKE_BASE=TRUE == MEM A DM<9>																MEM B DM<9> MAKE_BASE=TRUE == MEM B DM<9>															
MEM A DQ<79> MAKE_BASE=TRUE == MEM A DQ<79>																MEM B DQ<79> MAKE_BASE=TRUE == MEM B DQ<79>															
MEM A DQ<78> MAKE_BASE=TRUE == MEM A DQ<78>																MEM B DQ<78> MAKE_BASE=TRUE == MEM B DQ<78>															
MEM A DQ<77> MAKE_BASE=TRUE == MEM A DQ<77>																MEM B DQ<77> MAKE_BASE=TRUE == MEM B DQ<77>															
MEM A DQ<76> MAKE_BASE=TRUE == MEM A DQ<76>																MEM B DQ<76> MAKE_BASE=TRUE == MEM B DQ<76>															
MEM A DQ<75> MAKE_BASE=TRUE == MEM A DQ<75>																MEM B DQ<75> MAKE_BASE=TRUE == MEM B DQ<75>															
MEM A DQ<74> MAKE_BASE=TRUE == MEM A DQ<74>																MEM B DQ<74> MAKE_BASE=TRUE == MEM B DQ<74>															
MEM A DQ<73> MAKE_BASE=TRUE == MEM A DQ<73>																MEM B DQ<73> MAKE_BASE=TRUE == MEM B DQ<73>															
MEM A DQ<72> MAKE_BASE=TRUE == MEM A DQ<72>																MEM B DQ<72> MAKE_BASE=TRUE == MEM B DQ<72>															
MEM A DQ<71> MAKE_BASE=TRUE == MEM A DQ<71>																MEM B DQ<71> MAKE_BASE=TRUE == MEM B DQ<71>															
MEM A DQ<70> MAKE_BASE=TRUE == MEM A DQ<70>																MEM B DQ<70> MAKE_BASE=TRUE == MEM B DQ<70>															
MEM A DQ<69> MAKE_BASE=TRUE == MEM A DQ<69>																MEM B DQ<69> MAKE_BASE=TRUE == MEM B DQ<69>															
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MEM A DQ<67> MAKE_BASE=TRUE == MEM A DQ<67>																MEM B DQ<67> MAKE_BASE=TRUE == MEM B DQ<67>															
MEM A DQ<66> MAKE_BASE=TRUE == MEM A DQ<66>																MEM B DQ<66> MAKE_BASE=TRUE == MEM B DQ<66>															
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MEM A DQ<63> MAKE_BASE=TRUE == MEM A DQ<63>																MEM B DQ<63> MAKE_BASE=TRUE == MEM B DQ<63>															
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MEM A DQ<56> MAKE_BASE=TRUE == MEM A DQ<56>																MEM B DQ<56> MAKE_BASE=TRUE == MEM B DQ<56>															
CPU CHANNEL A DQS 10 -> DIMM A DQS 10																CPU CHANNEL B DQS 10 -> DIMM B DQS 10															
MEM A DQS N<10> MAKE_BASE=TRUE == MEM A DQS N<10>																MEM B DQS N<10> MAKE_BASE=TRUE == MEM B DQS N<10>															
MEM A DQS P<10> MAKE_BASE=TRUE == MEM A DQS P<10>																MEM B DQS P<10> MAKE_BASE=TRUE == MEM B DQS P<10>															
MEM A DM<10> MAKE_BASE=TRUE == MEM A DM<10>																MEM B DM<10> MAKE_BASE=TRUE == MEM B DM<10>															
MEM A DQ<87> MAKE_BASE=TRUE == MEM A DQ<87>																MEM B DQ<87> MAKE_BASE=TRUE == MEM B DQ<87>															
MEM A DQ<86> MAKE_BASE=TRUE == MEM A DQ<86>																MEM B DQ<86> MAKE_BASE=TRUE == MEM B DQ<86>															
MEM A DQ<85> MAKE_BASE=TRUE == MEM A DQ<85>																MEM B DQ<85> MAKE_BASE=TRUE == MEM B DQ<85>															
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MEM A DQ<82> MAKE_BASE=TRUE == MEM A DQ<82>																MEM B DQ<82> MAKE_BASE=TRUE == MEM B DQ<82>															
MEM A DQ<81> MAKE_BASE=TRUE == MEM A DQ<81>																MEM B DQ<81> MAKE_BASE=TRUE == MEM B DQ<81>															
MEM A DQ<80> MAKE_BASE=TRUE == MEM A DQ<80>																MEM B DQ<80> MAKE_BASE=TRUE == MEM B DQ<80>															
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MEM A DQ<57> MAKE_BASE=TRUE == MEM A DQ<57>																MEM B DQ<57> MAKE_BASE=TRUE == MEM B DQ<57>															
MEM A DQ<56> MAKE_BASE=TRUE == MEM A DQ<56>																															



Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMM_SCL
- =I2C_SODIMM_SDA

BOM options provided by this page:
(NONE)

DDR3 DECOUPL

EVENLY AT CONNECTOR)

D

D

C

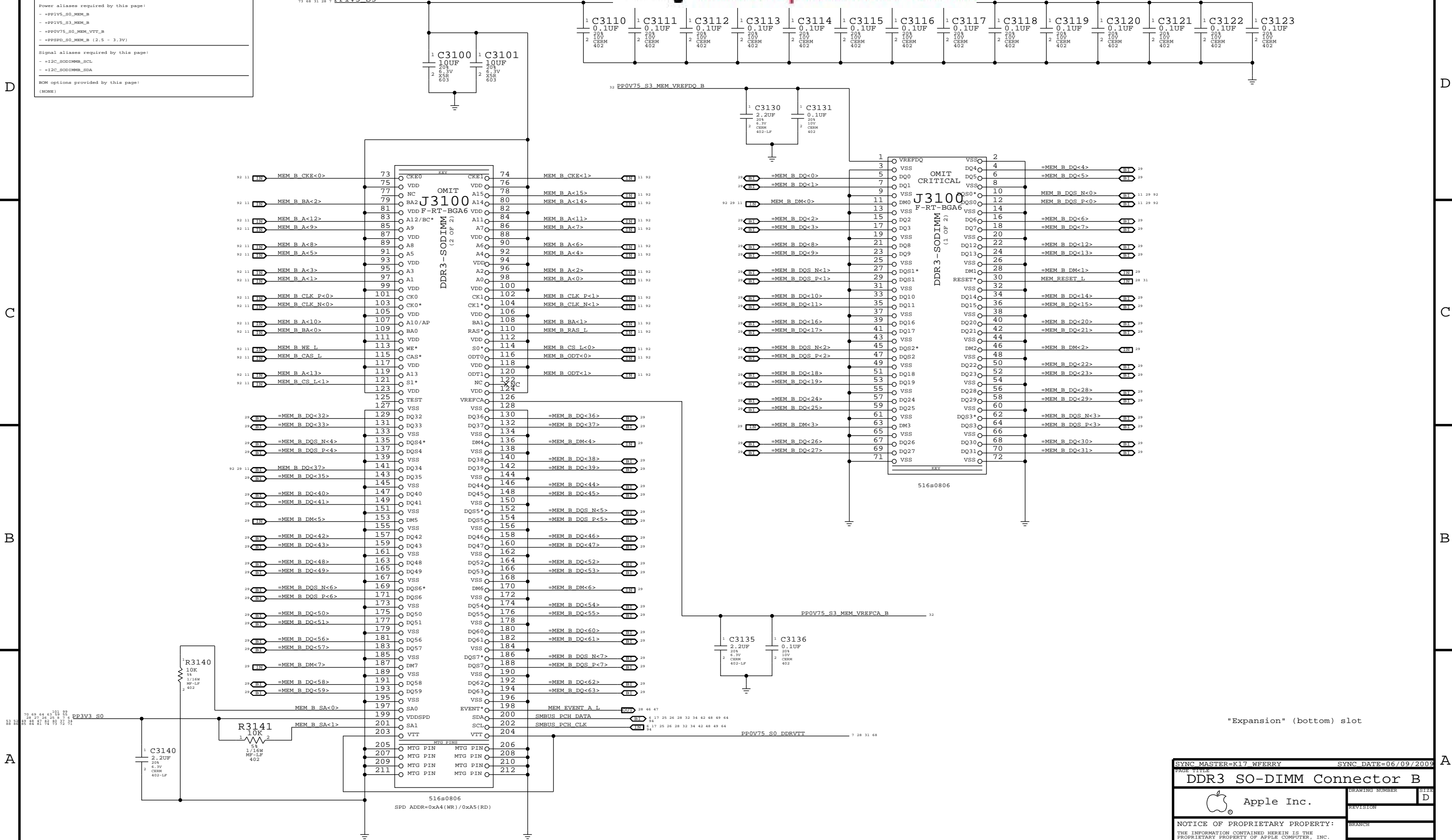
C

B

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A

A



"Expansion" (bottom) slot

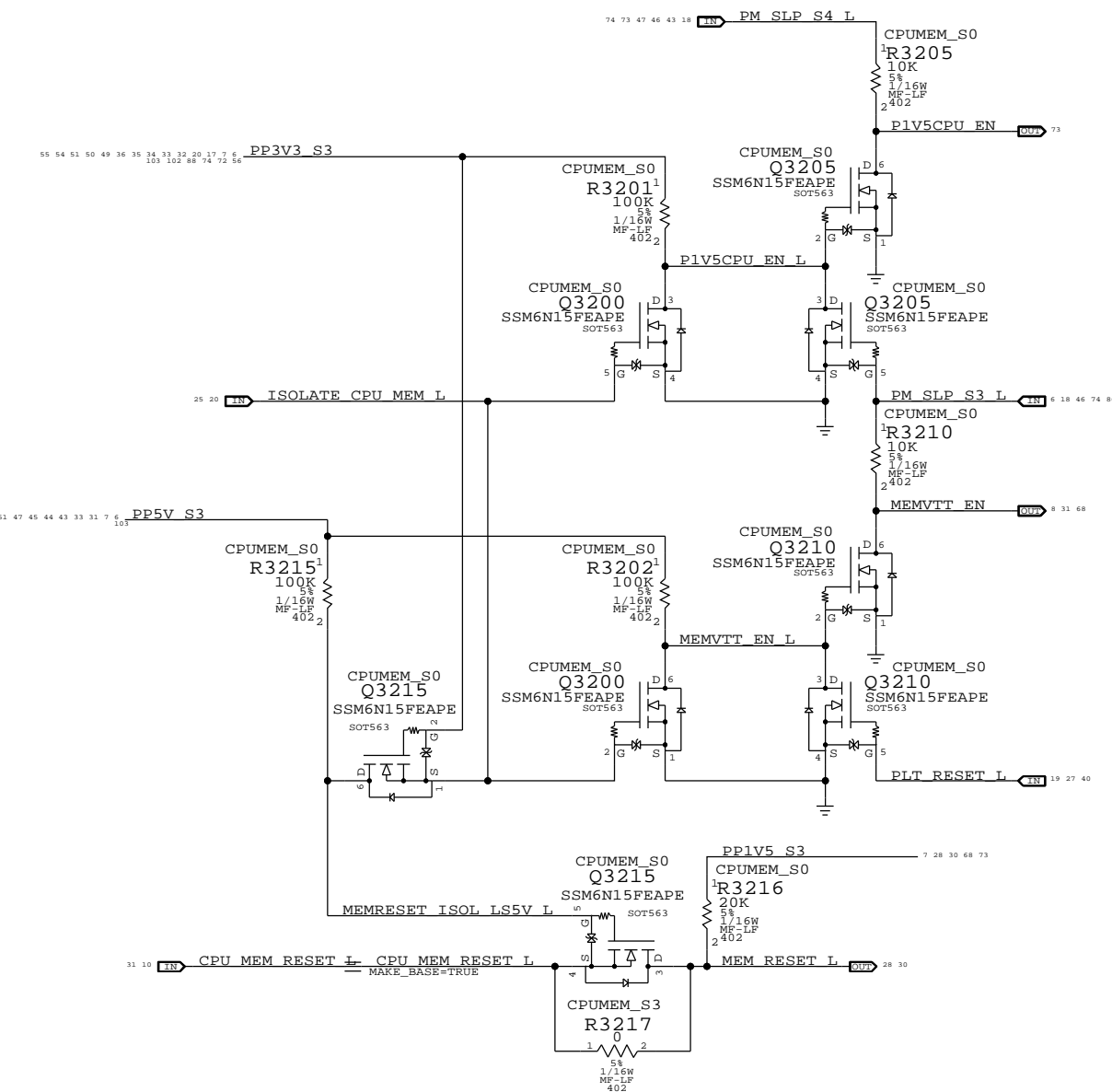
SYNC MASTER=K17.WFERRY		SYNC DATE=06/09/2009	
PAGE TITLE DDR3 SO-DIMM Connector B			
Apple Inc.		DRAWING NUMBER	SIZE D
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		PAGE 31 OF 132	SHEET 30 OF 103



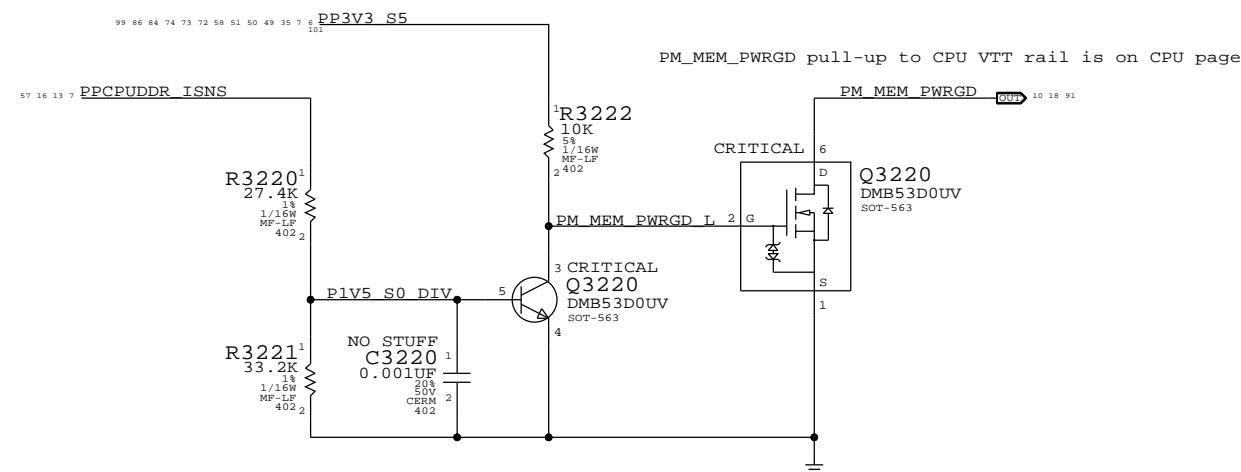
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L

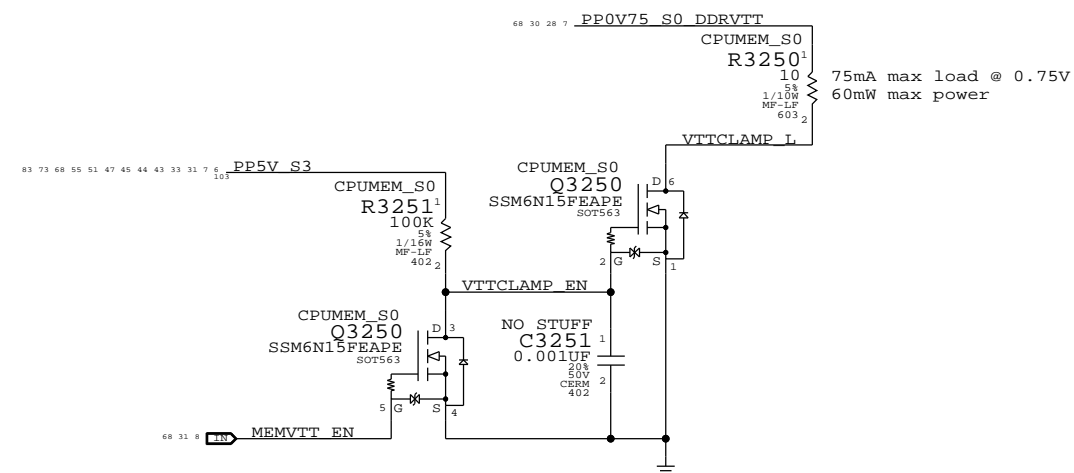


1V5 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3



Step	ISOLATE_CPU_MEM_L	PLT_RST_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1	1
2	0	0	1	1	1	1	0	1
3	0	0	0	1	X	1	0	0
4	0	0	1	1	X	1	0	1
5	0	1	1	1	0 (*)	1	1	1
6	0	1	1	1	1	1	1	1
to	1	1	1	1	1	CPU_MEM_RESET_L	1	1
S0	7							

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

SYNC MASTER=K18 MLB		SYNC DATE=10/14/2009	
PAGE TITLE			
CPU Memory S3 Support			
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NOTE: Must not enable more than two SO-DIMM margining buffers at once or VRef source may be overloaded.

D

C

B

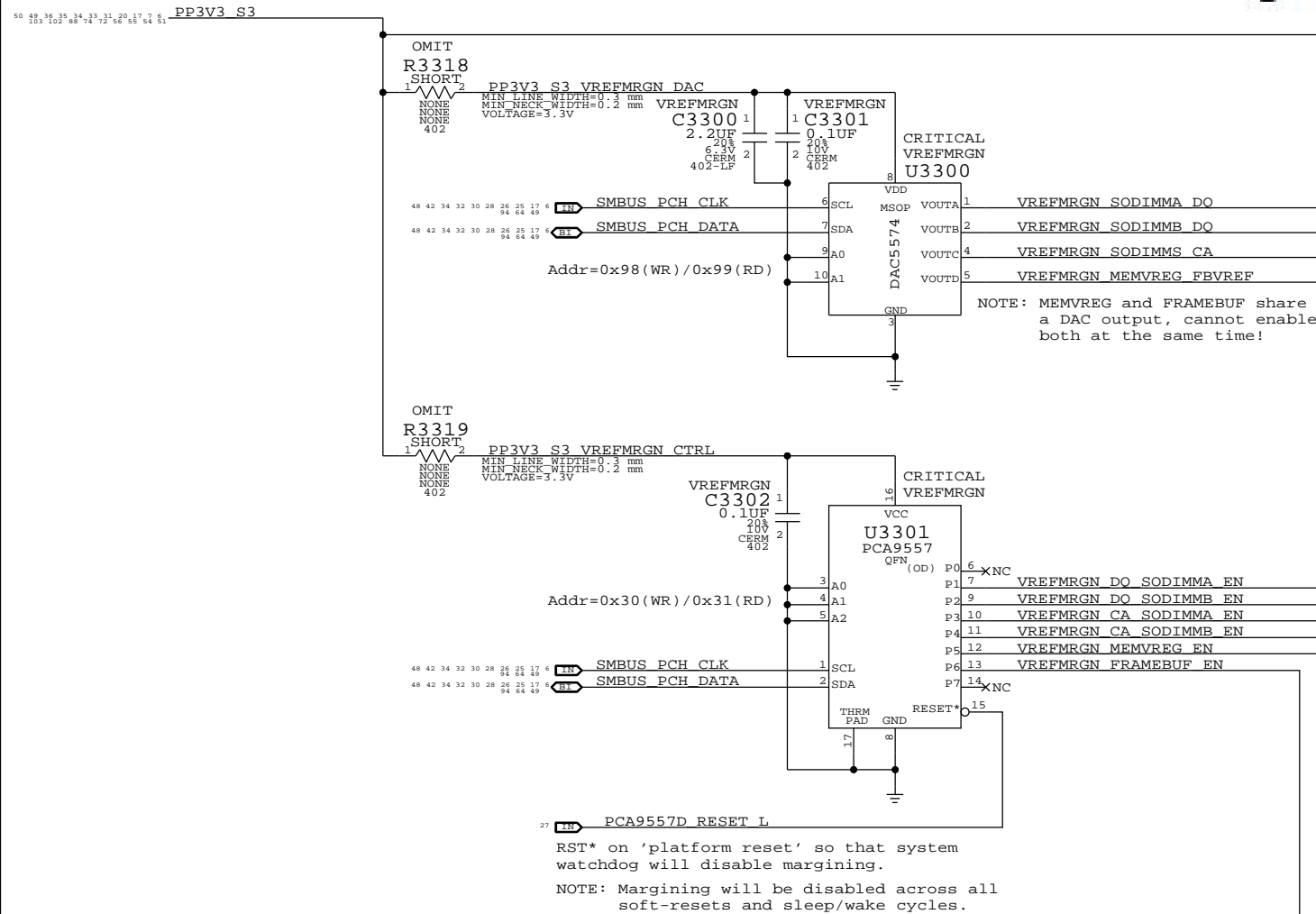
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Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0.5%,0402,SM,LF	R3303,R3305		VREFMRGN_NOT
116S0004	2	RES,MTL FILM,0.5%,0402,SM,LF	R3309,R3311		VREFMRGN_NOT

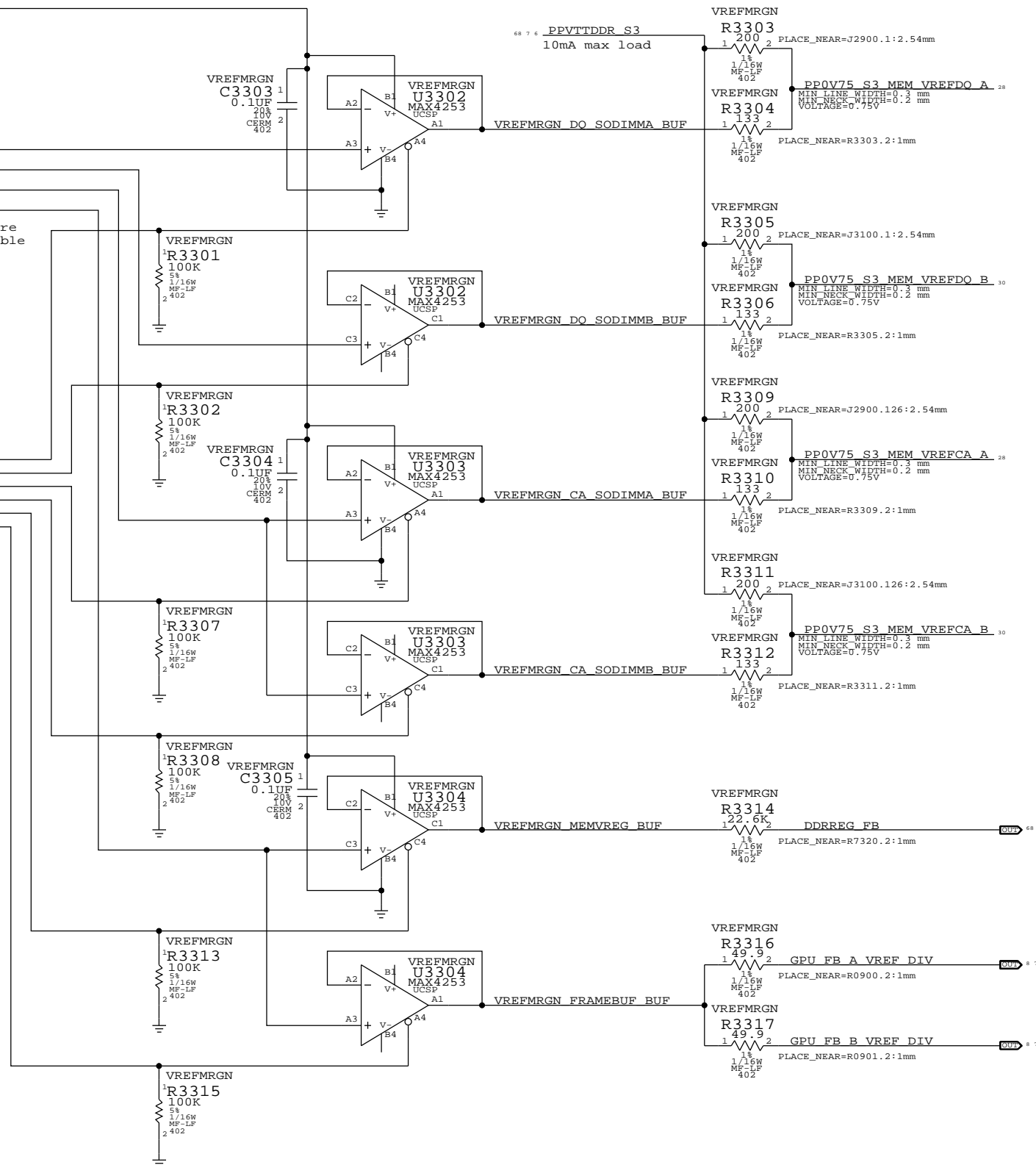
Page Notes


Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF

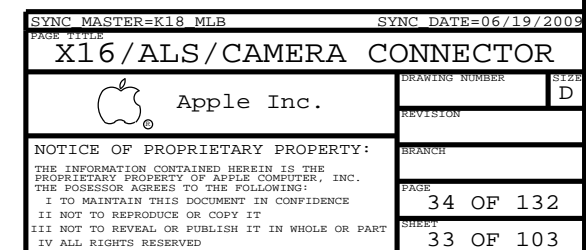
Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN - Stuffs VREF Margining Circuitry.
VREFMRGN_NOT - Bypasses VREF Margining Circuitry.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% Vref)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value			0.75V (DAC: 0x3A)		1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:			0.300V - 1.200V (+/- 450mV)		1.998V - 1.002V (+/- 498mV)	1.056V - 1.442V (+/- 180mV)
DAC range:			0.000V - 1.501V (0x00 - 0x74)		0.000V - 1.501V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
Vref current:			+3.4mA - -3.4mA (- = sourced)		+33uA - -33uA (- = sourced)	+6.0mA - -3.0mA (- = sourced)
DAC step size:			7.69mV / step @ output		8.59mV / step @ output	1.51mV / step @ output



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FSB/DDR3/FRAMEBUF Vref Margining			
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EXPRESSCARD/34 FLEX CONNECTOR

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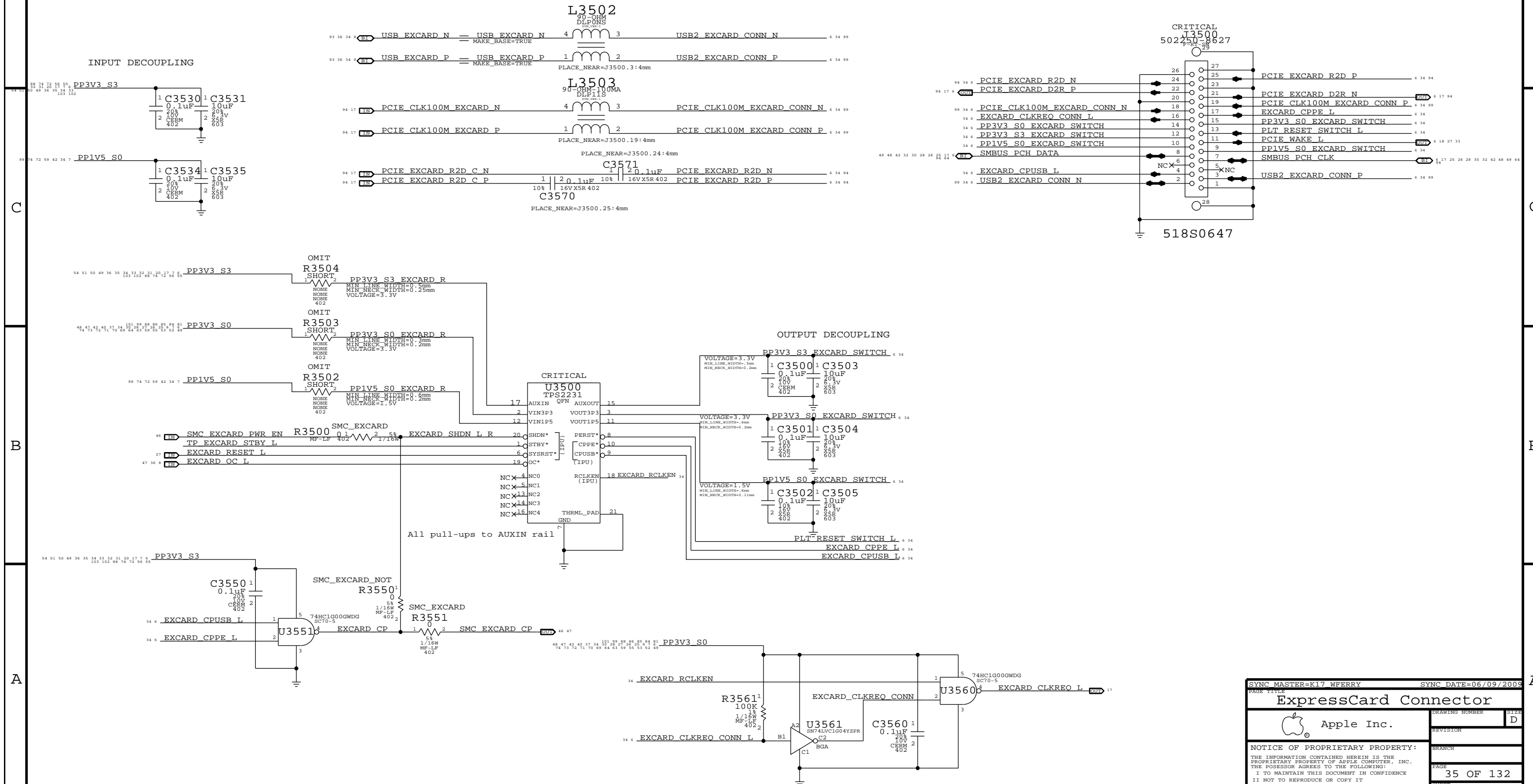
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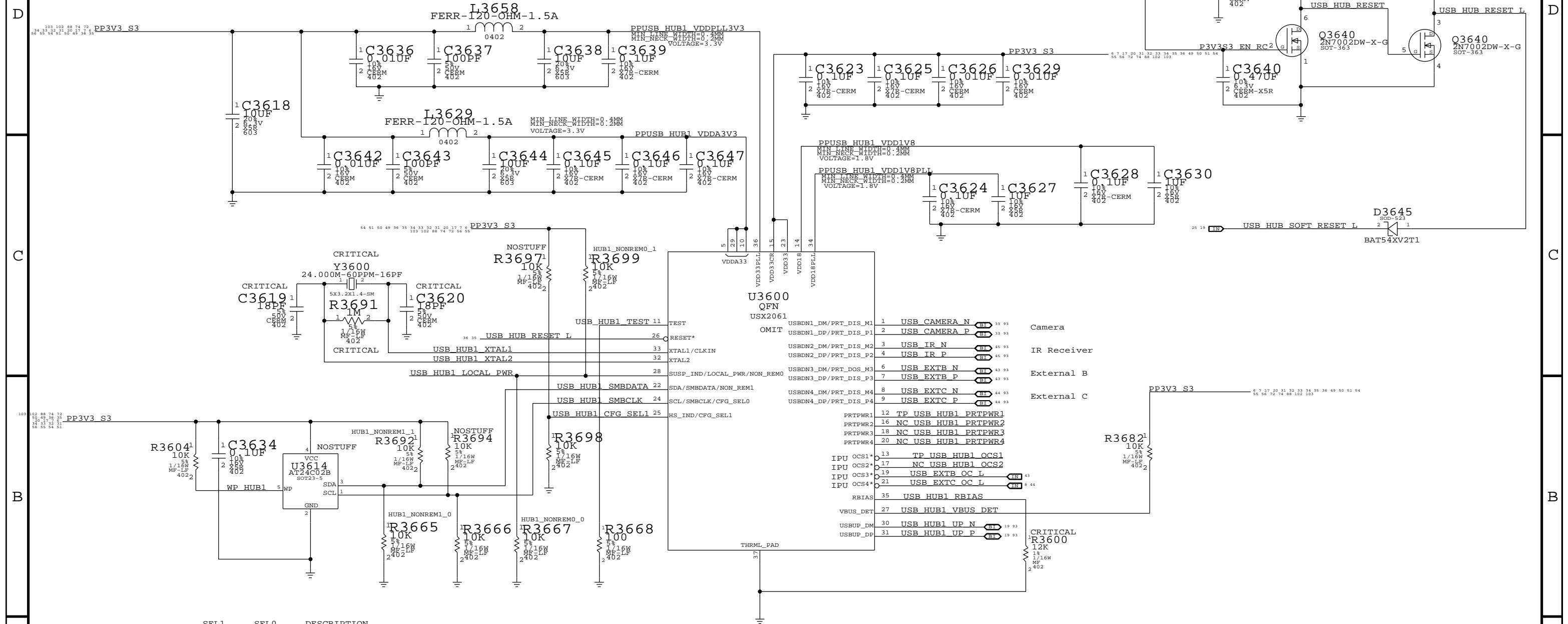
A



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ExpressCard Connector			
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USE



SEL1	SEL0	DESCRIPTION
0	0	Internal Default with Self powered Operation
0	1	SMBUS Slave Config
1	0	Internal Default with Bus powered Operation
1	1	EEPROM Supported

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0720	2	IC,ASSP,USB2.0,HUB CTRL,4 PRT,160P	U3600,U3700	CRITICAL	USBHUB_2514
338S0824	2	IC,USB2.0,USB 2.0,HUB CTRL,4 PRT,160P	U3600,U3700	CRITICAL	USBHUB_2514B
338S0721	2	IC,USX2061,USB 2.0,HUB CTRL,4 PRT,160P	U3600,U3700	CRITICAL	USBHUB_2061

BOM GROUP	BOM OPTIONS
HUB1_ALLREM	HUB1_NONREM1_0,HUB1_NONREM0_0
HUB1_1NONREM	HUB1_NONREM1_0,HUB1_NONREM0_1
HUB1_2NONREM	HUB1_NONREM1_1,HUB1_NONREM0_0
HUB1_3NONREM	HUB1_NONREM1_1,HUB1_NONREM0_1

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are Non removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2 and 3 are non Removable

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USB HUB 1

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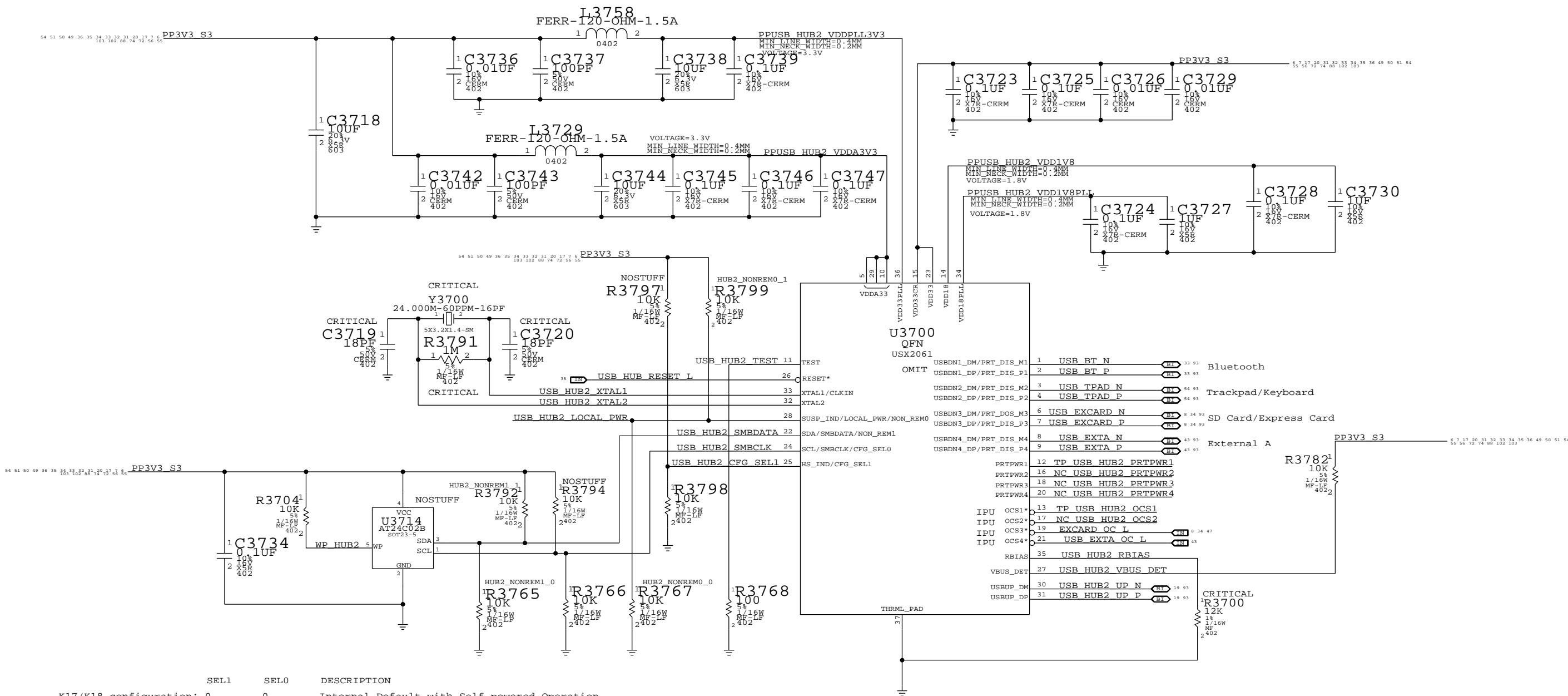
SHEET

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USB HUB-2



	SEL1	SEL0	DESCRIPTION
K17/K18 configuration:	0	0	Internal Default with Self powered Operation
	0	1	SMBUS Slave Config
	1	0	Internal Default with Bus powered Operation
	1	1	EEPROM Supported

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

BOM GROUP	BOM OPTIONS
HUB2_ALLREM	HUB2_NONREM0_0, HUB2_NONREM0_0
HUB2_1NONREM	HUB2_NONREM1_0, HUB2_NONREM0_1
HUB2_2NONREM	HUB2_NONREM1_1, HUB2_NONREM0_0
HUB2_3NONREM	HUB2_NONREM1_1, HUB2_NONREM0_1

SYNC MASTER=K18 MLB SYNC DATE=10/09/2009

USB HUB 2

Apple Inc.

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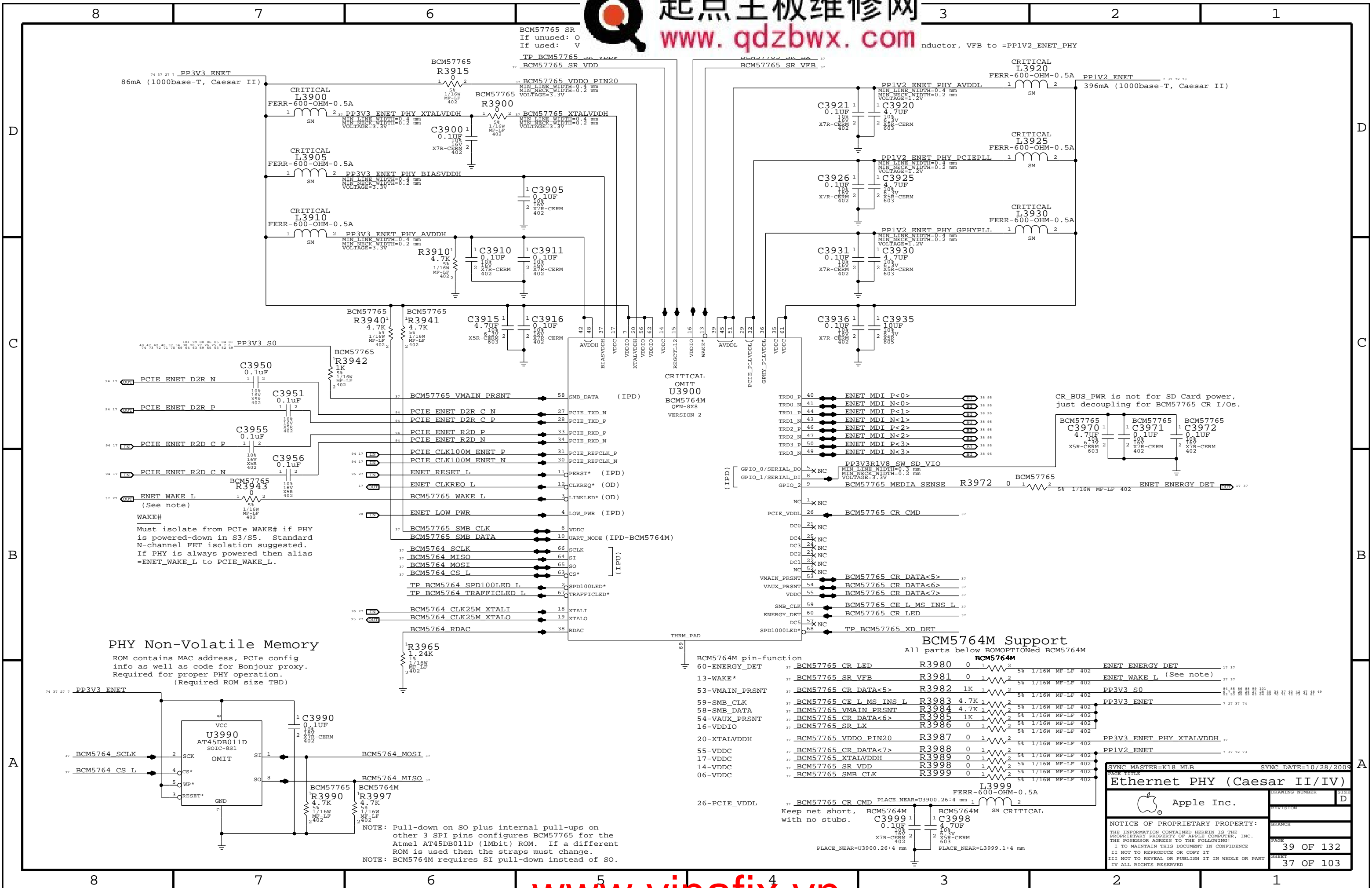
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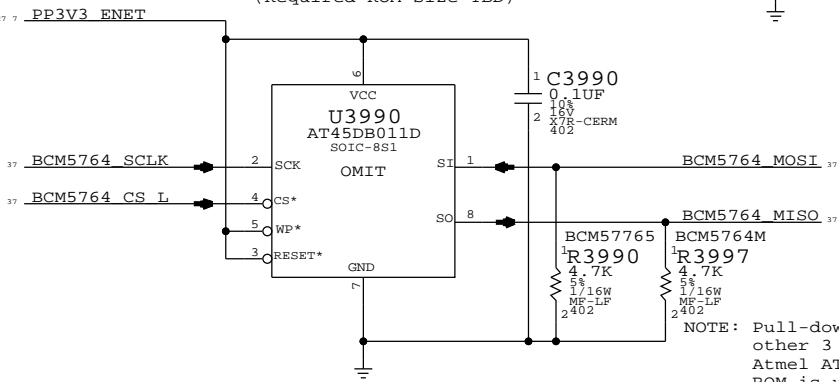
PAGE
37 OF 132

SHEET
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PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy. Required for proper PHY operation. (Required ROM size TBD)



NOTE: Pull-down on S0 plus internal pull-ups on other 3 SPI pins configures BCM57765 for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: BCM5764M requires SI pull-down instead of S0.

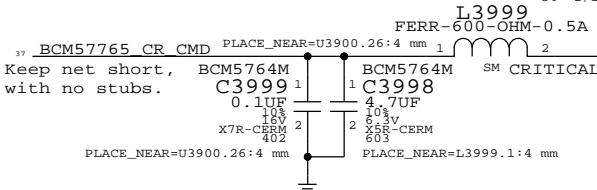
BCM5764M pin-function

- 60-ENERGY_DET
- 13-WAKE*
- 53-VMMAIN_PRSENT
- 59-SMB_CLK
- 58-SMB_DATA
- 54-VAUX_PRSENT
- 16-VDDIO
- 20-XTALVDDH
- 55-VDDC
- 17-VDDC
- 14-VDDC
- 06-VDDC
- 26-PCIE_VDDL

BCM5764M Support

All parts below BOMOPTIONED BCM5764M

BCM5764M		BCM5764M	
BCM57765 CR LED	R3980	0	1/16W MF-LF 402
BCM57765 SR VFB	R3981	0	1/16W MF-LF 402
BCM57765 CR DATA<5>	R3982	1K	1/16W MF-LF 402
BCM57765 CE L MS INS L	R3983	4.7K	1/16W MF-LF 402
BCM57765 VMMAIN_PRSENT	R3984	4.7K	1/16W MF-LF 402
BCM57765 CR DATA<6>	R3985	1K	1/16W MF-LF 402
BCM57765 SR LX	R3986	0	1/16W MF-LF 402
BCM57765 VDDO PIN20	R3987	0	1/16W MF-LF 402
BCM57765 CR DATA<7>	R3988	0	1/16W MF-LF 402
BCM57765 XTALVDDH	R3989	0	1/16W MF-LF 402
BCM57765 SR VDD	R3990	0	1/16W MF-LF 402
BCM57765 SMB_CLK	R3991	0	1/16W MF-LF 402



SYNC MASTER=K18 MLB

SYNC DATE=10/28/2009

Ethernet PHY (Caesar II/IV)

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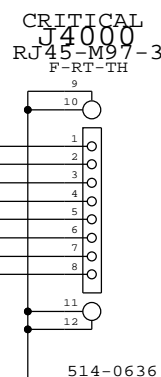
SIZE

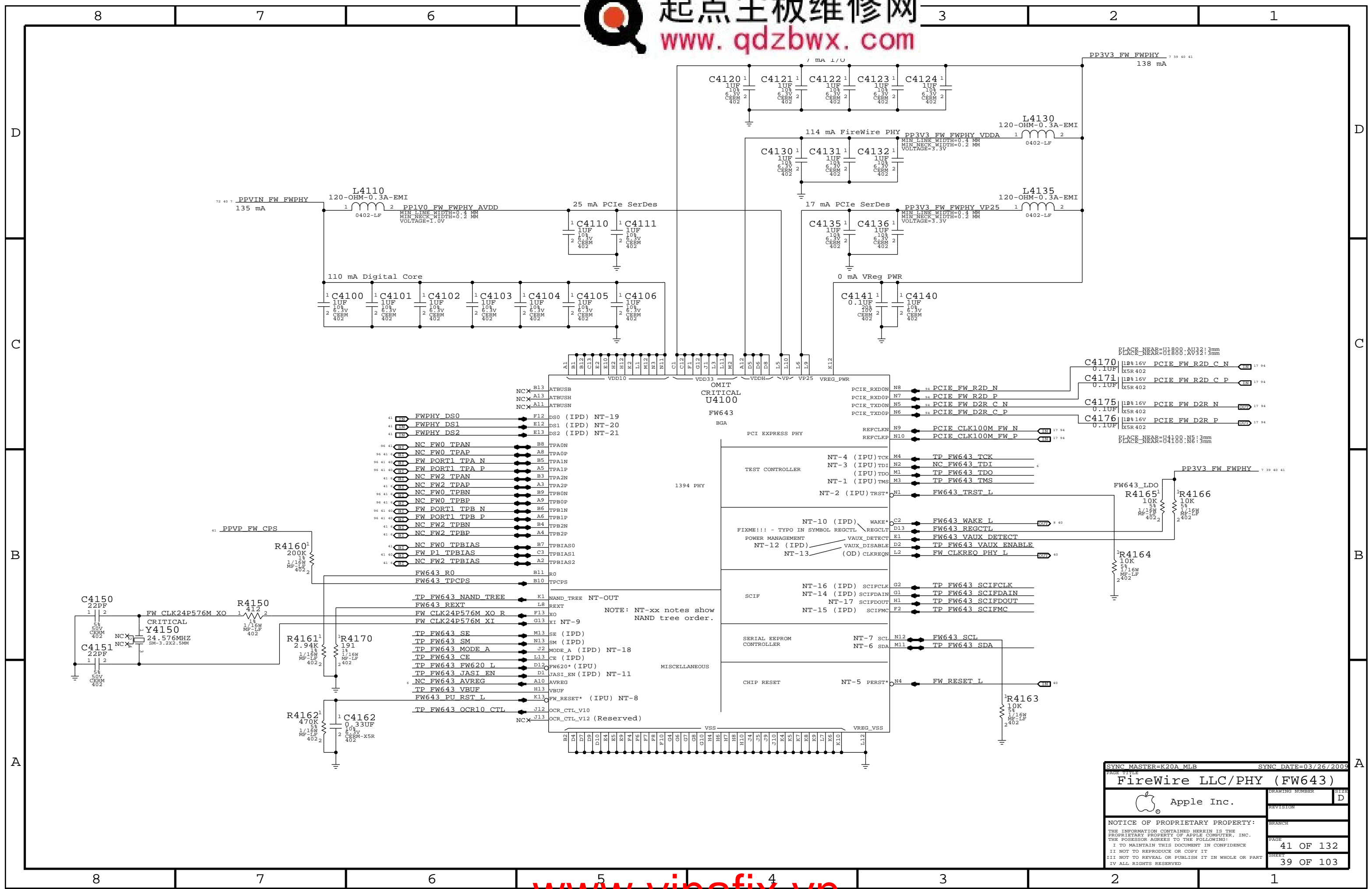
D

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Power aliases required by this page: (NONE)
Signal aliases required by this page: (NONE)
BOM options provided by this page: (NONE)



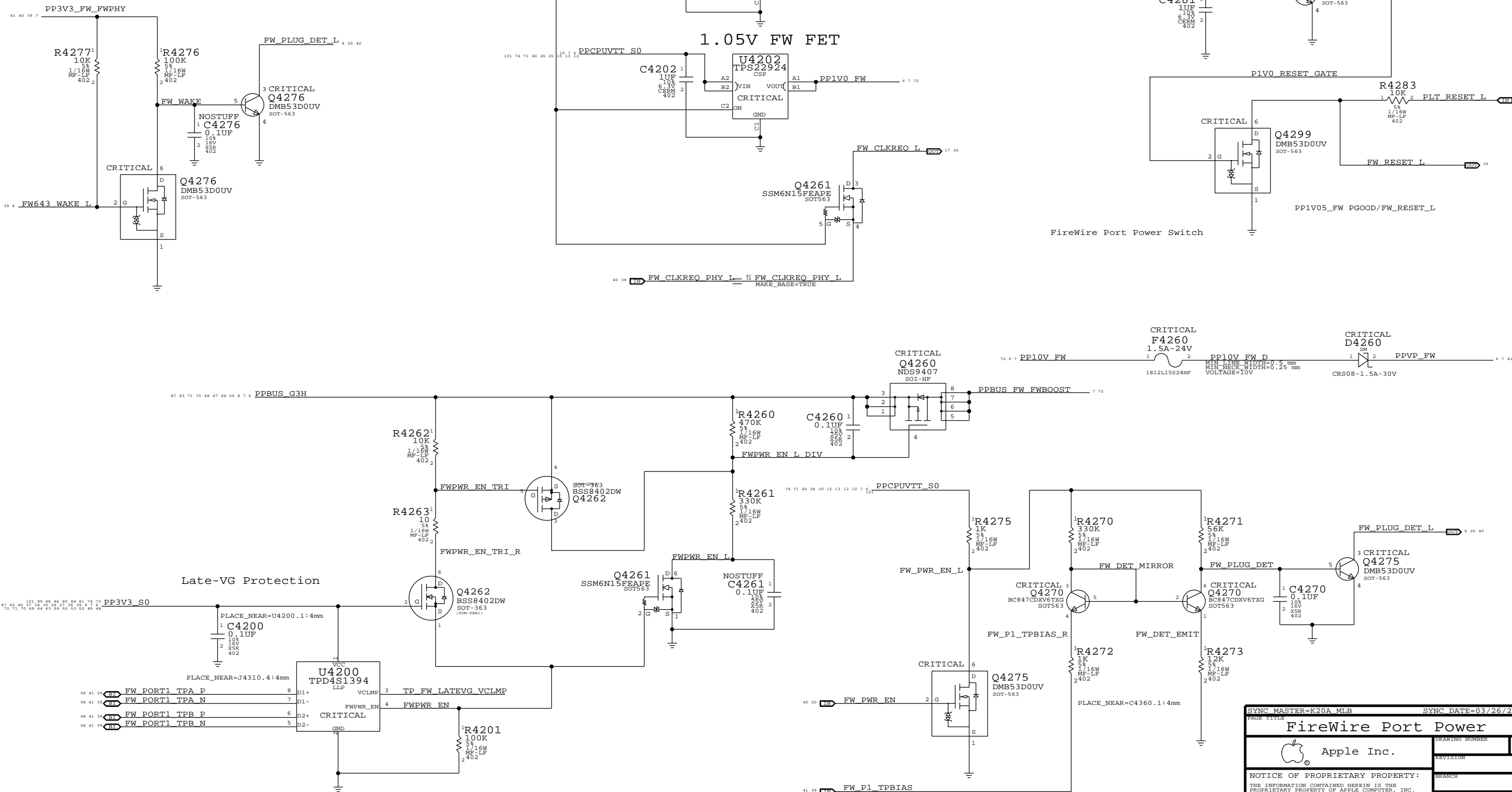



SYNC MASTER=K20A MLB		SYNC DATE=03/26/2009	
PAGE TITLE		FireWire LLC/PHY (FW643)	
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Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (system supply for bus power)
- =PP3V3_FW_LATEVG_ACTIVE
- =PPVP_FW_SUMNODE (power passthru summation node)
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
- FW_PORT_FAULT_PU



SYNC MASTER=K20A_MLB		SYNC DATE=03/26/2009	
PAGE TITLE			
FireWire Port Power			
 Apple Inc.		DRAWING NUMBER	SIZE D
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Page Notes

Power aliases required by this page:

- =PPVP_FW_PORT1
- =PP3V3_FW_LATEVG

Signal aliases required by this page:

(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:

(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple

FireWire Design Guide (FWDG 0.6, 5/14/03)

FireWire PHY Config Straps

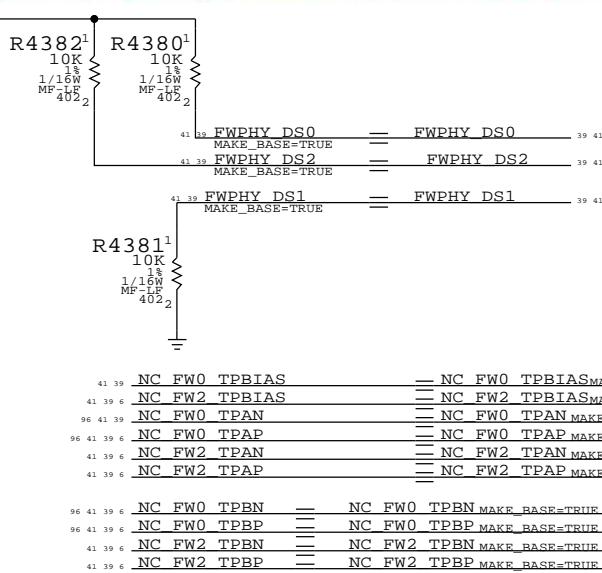
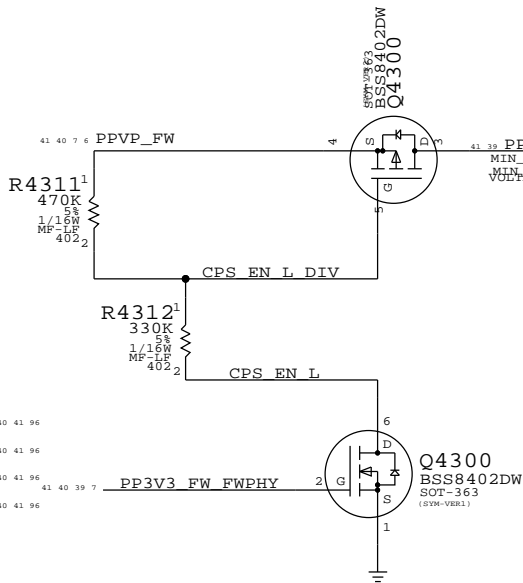
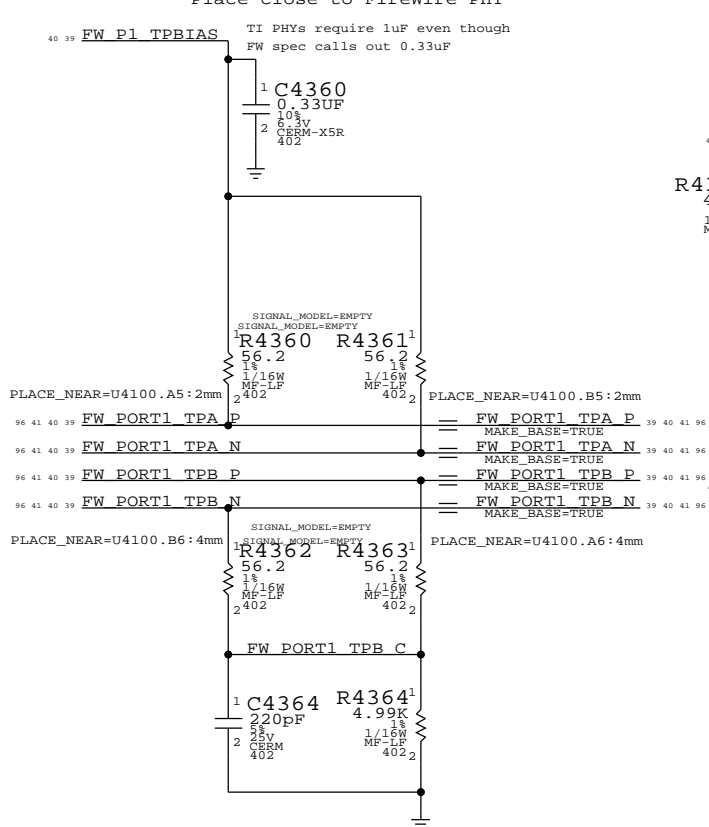
Configures PHY for:

- 1-port Portable Power Class (0)

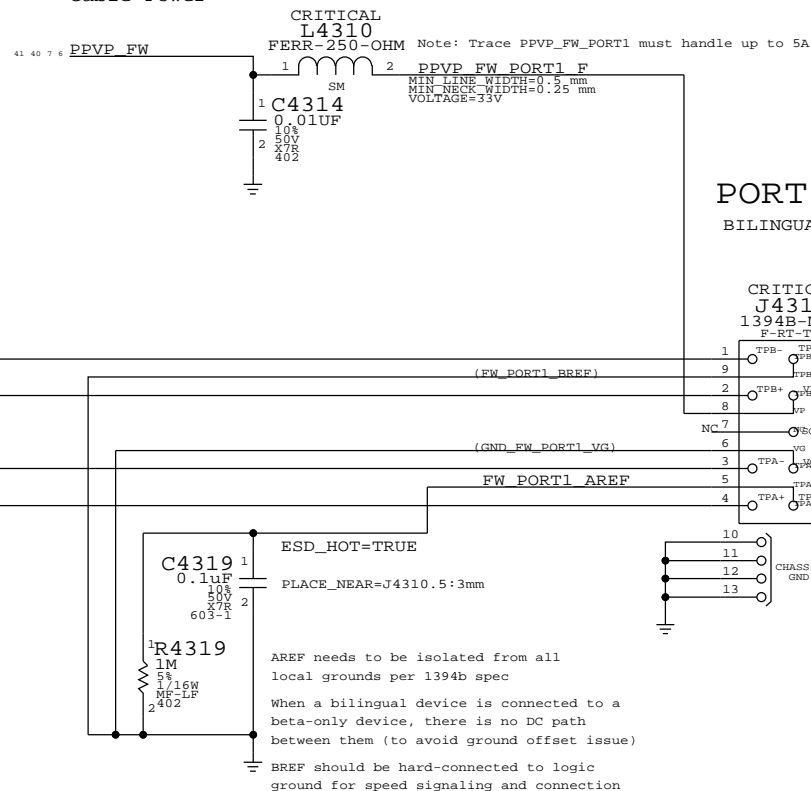
- Port "1" Bilingual (1394B)

Termination

Place close to FireWire PHY

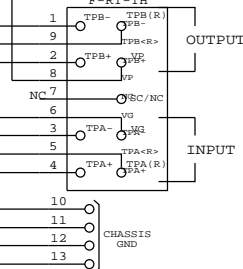


Cable Power



PORT 1 BILINGUAL

CRITICAL J4310 1394B-M97 F-RT-TH



514S0605

SYNC MASTER=K18_MLB		SYNC DATE=07/08/2009	
PAGE TITLE		FireWire Ports	
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NOTE: 3.3V must be S0 if 5V is S3 or S5 to ensure the drive is unpowered in S3/S5.

PP3V3_S0

PP3V3_S0

PP3V3_S0

PP3V3_S0

PP3V3_S0

PP3V3_S0

PP3V3_S0

PP3V3_S0

PP3V3_S0

PP3V3_S0

PP3V3_S0

PP3V3_S0

PP3V3_S0

PP3V3_S0

PP3V3_S0

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PP3V3_S0

PP3V3_S0

PP3V3_S0

PP3V3_S0

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PP3V3_S0

PP3V3_S0

SATA ODD Port

SATA HDD Port

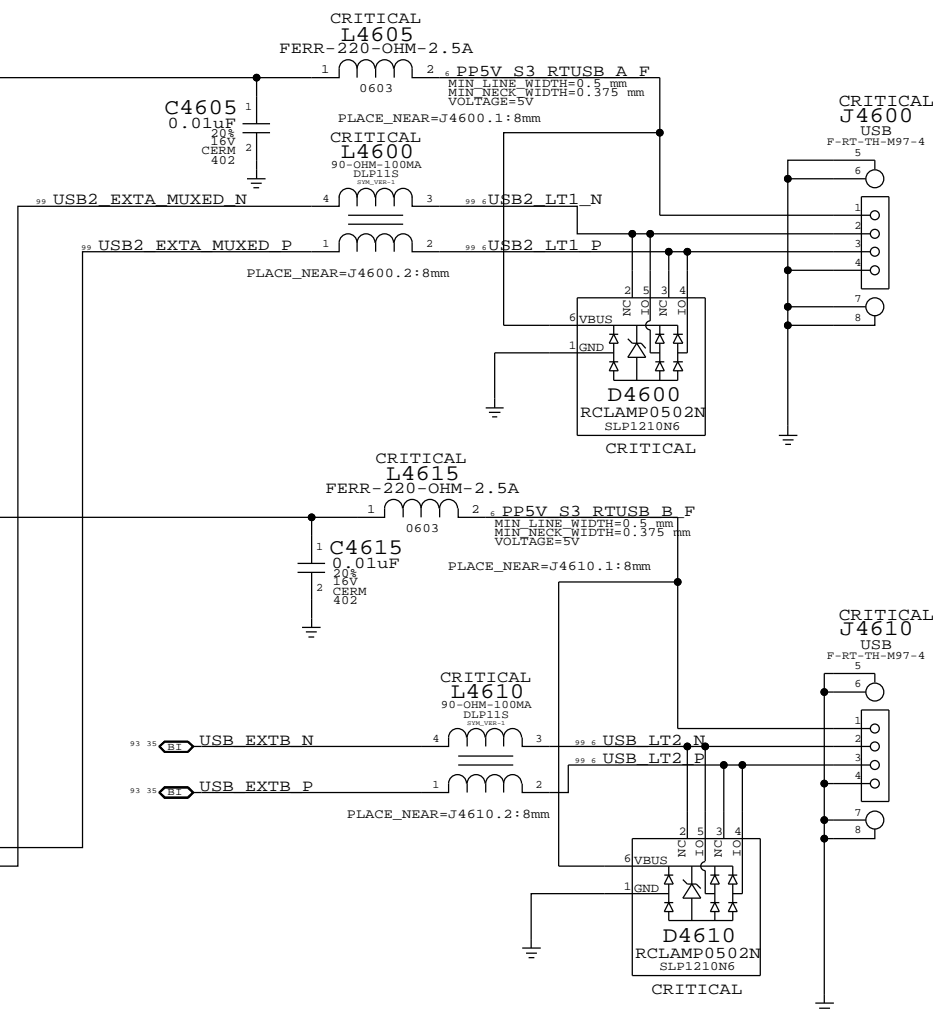
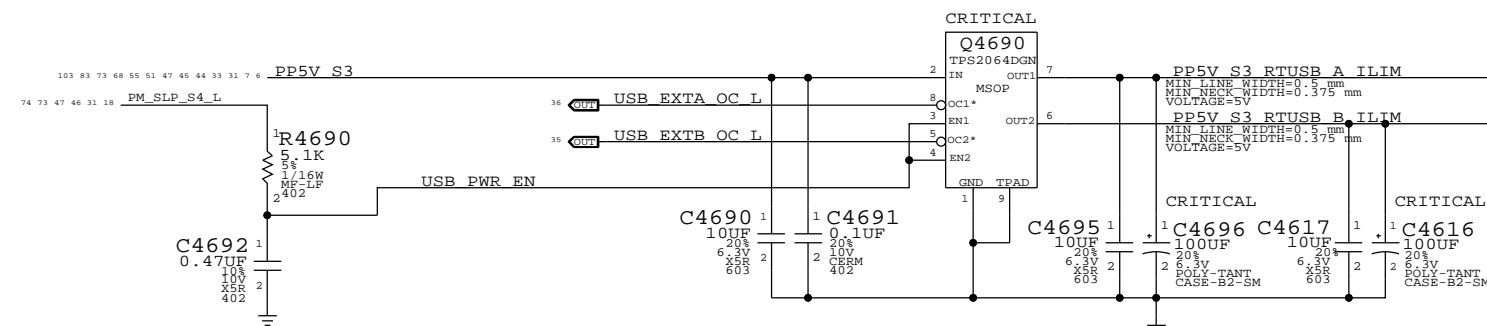
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0769	1	SATA 3GB/S REDRIVER, LOW POWER	U4510	CRITICAL	RDRV_8511
338S0778	1	SATA 3GB/S REDRIVER, LOW POWER	U4510	CRITICAL	RDRV_8515_A1
338S0848	1	SATA 3GB/S REDRIVER, LOW POWER	U4510	CRITICAL	RDRV_8515_A2

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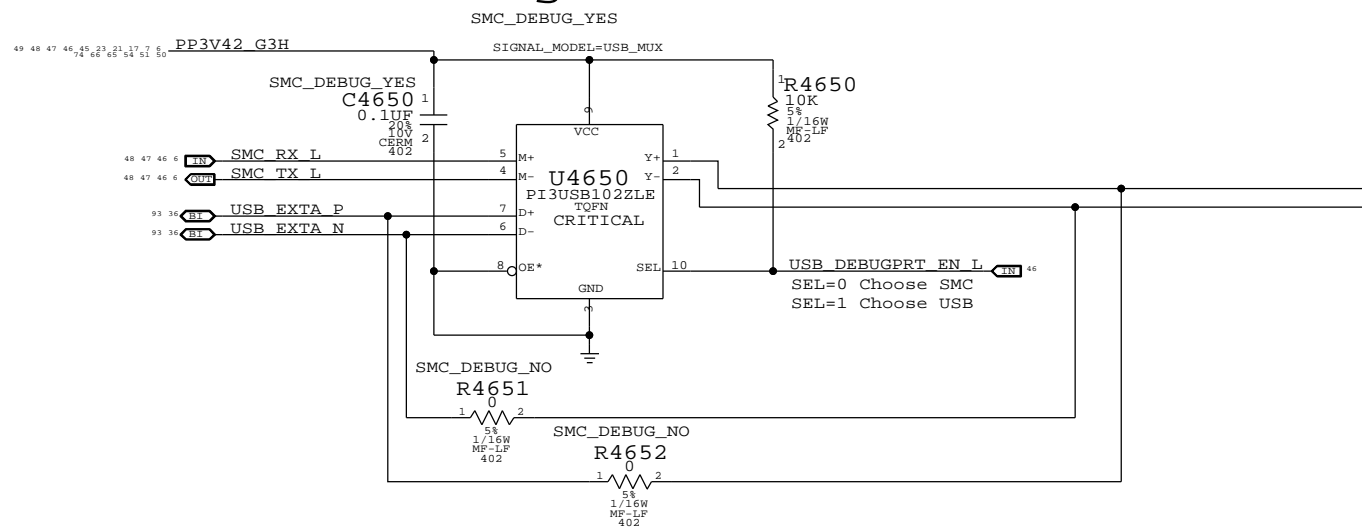


Port Power Switch


Left USB Port A



USB/SMC Debug Mux



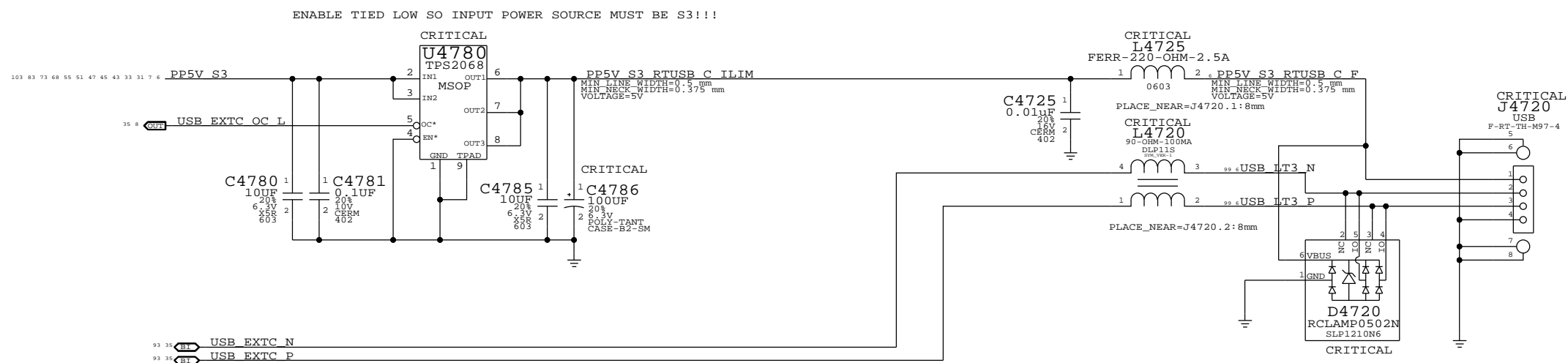
Left USB Port B


SYNC MASTER=K17 WFERRY		SYNC DATE=06/09/2009	
PAGE			
External USB Connectors			
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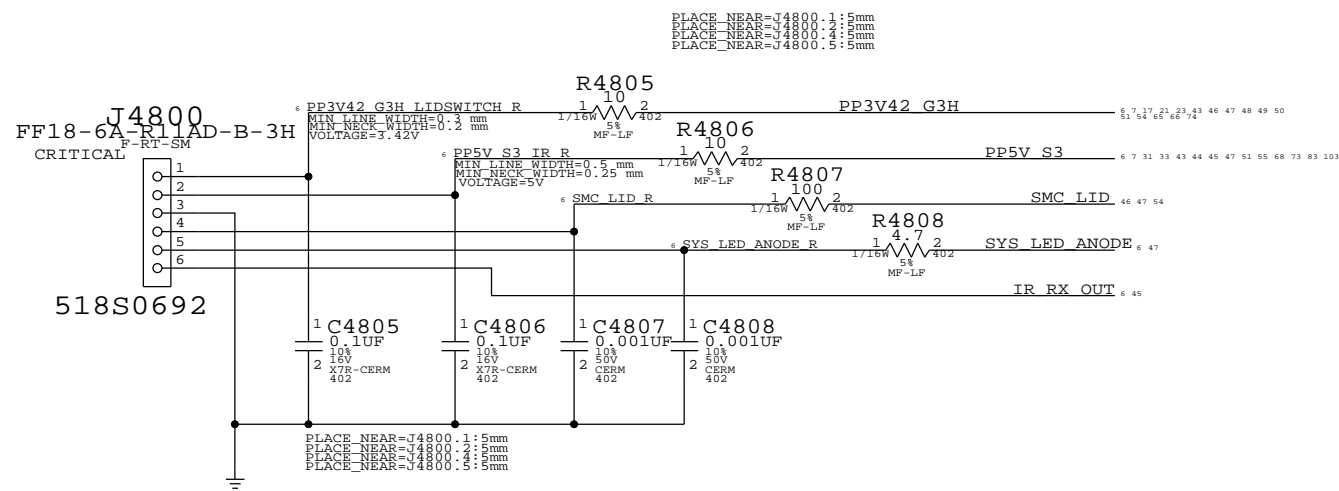
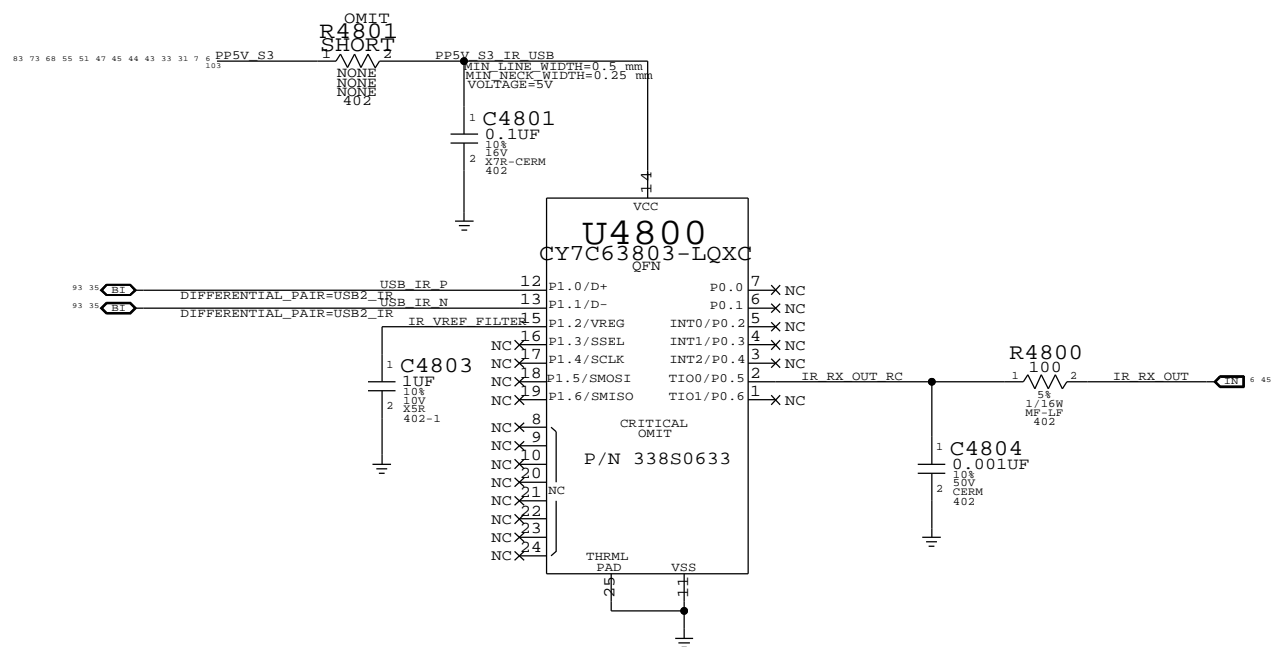



Port Power Switch

LEFT USB PORT C



SYNC MASTER=K20A MLB		SYNC DATE=03/26/2009	
PAGE 1			
PROJECT SPECIFIC CONNS			
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		REVISION	D
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SYNC MASTER=K20A MLB		SYNC DATE=03/26/2009	
PAGE TITLE			
Front Flex Support		DRAWING NUMBER	SIZE
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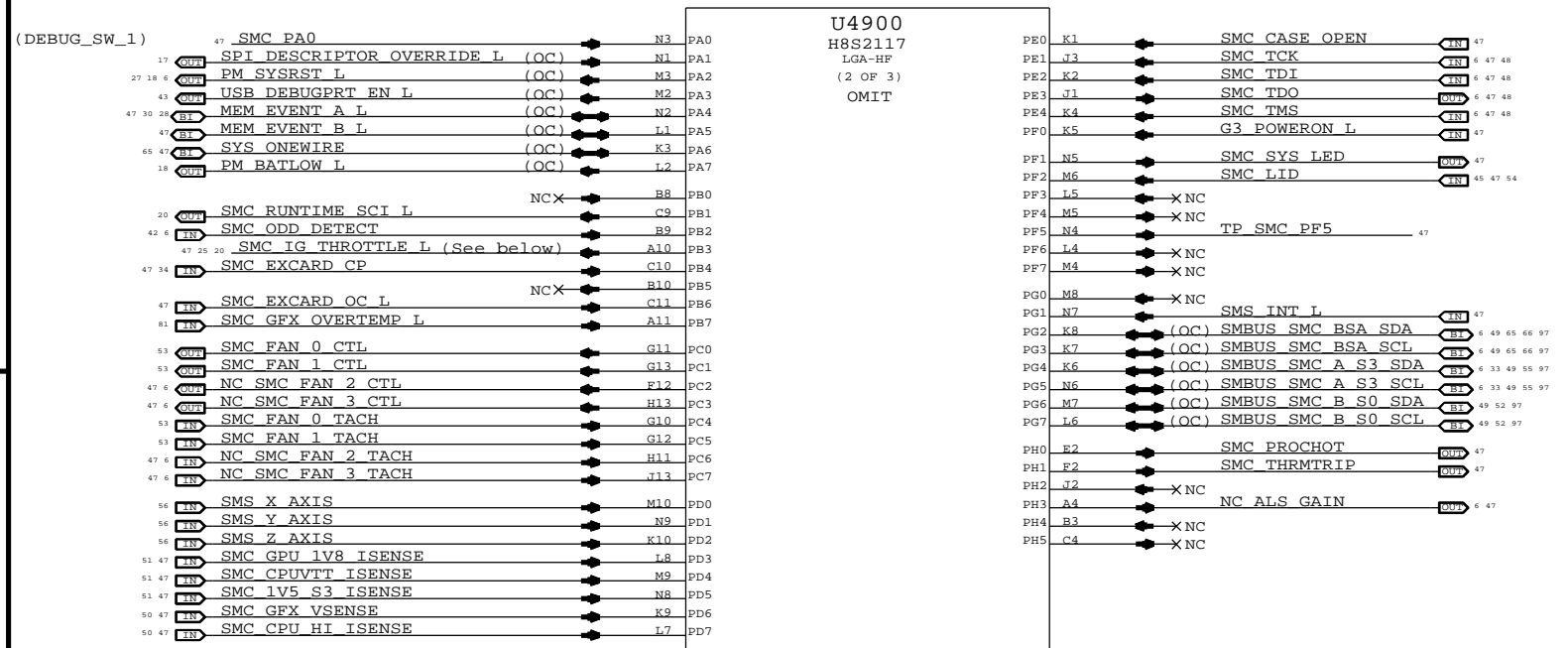
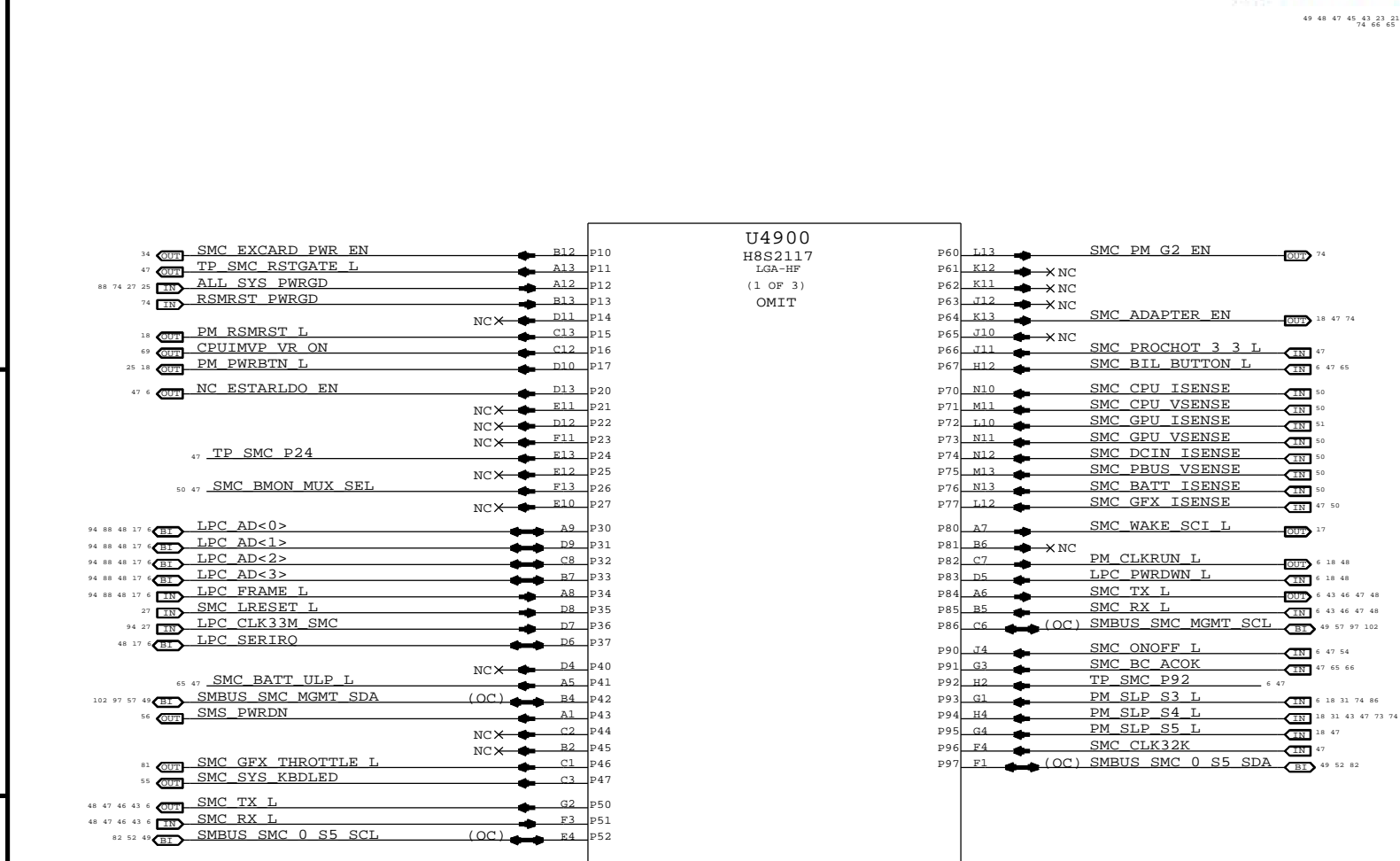
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

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SMC_PB3:
SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)

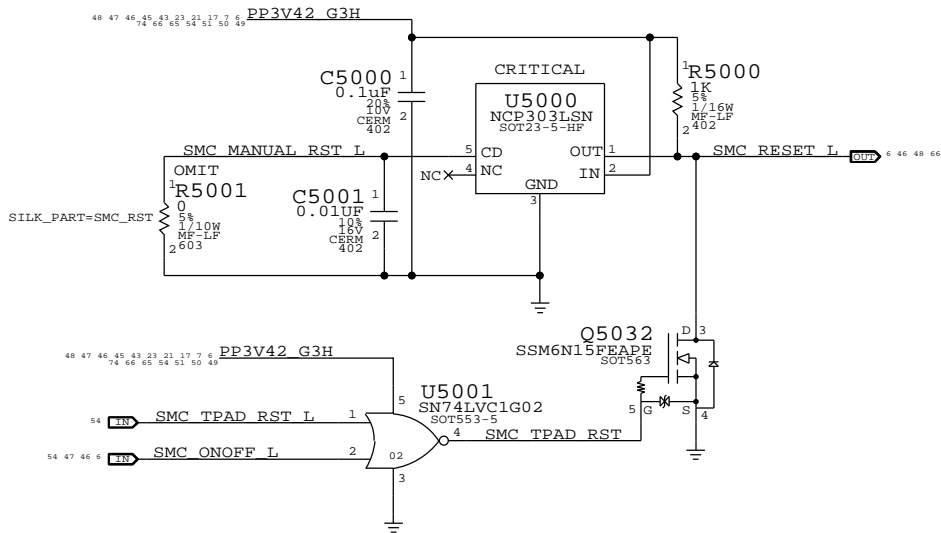
NOTE: P94 and P95 are shorted, P95 could be spare.

NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

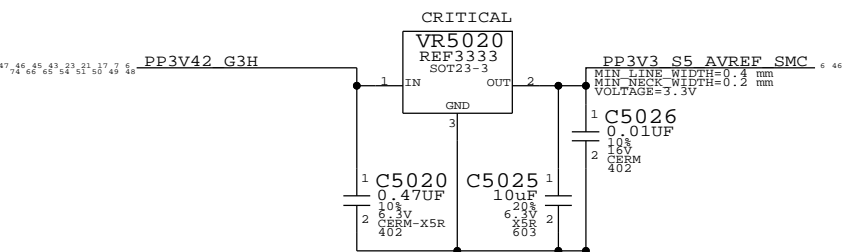
SYNC MASTER=K17.WFERRY		SYNC DATE=06/09/2009	
PAGE TITLE			
SMC		DRAWING NUMBER	SIZE
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SMC Reset "Button" / Brownout Detect

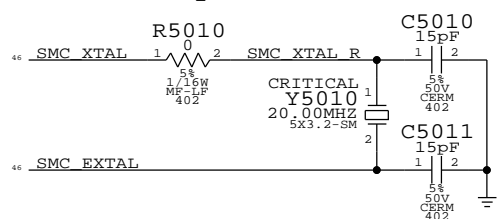


SMC AVREF Supply

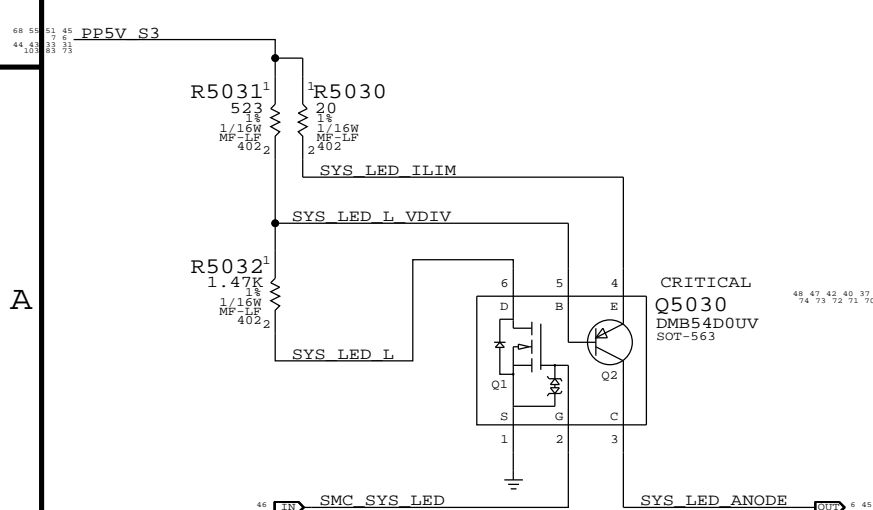


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1912		ALL	Interall ISL60002-33

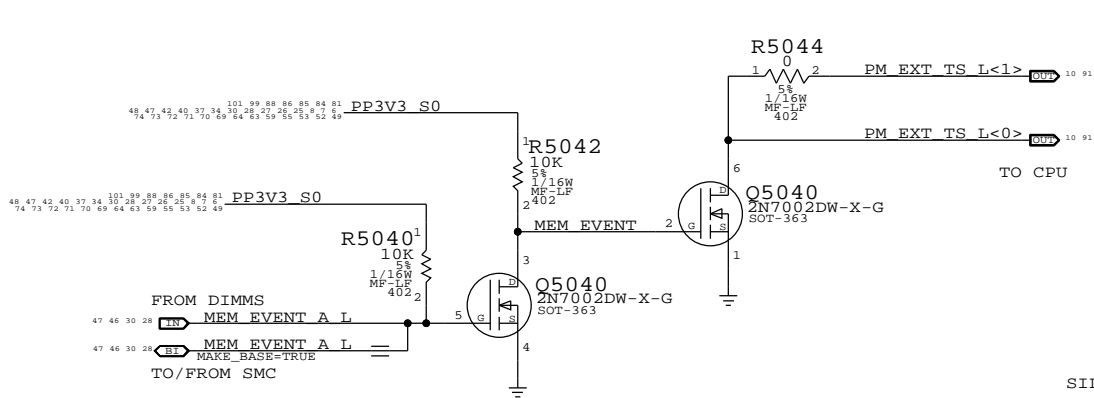
SMC Crystal Circuit



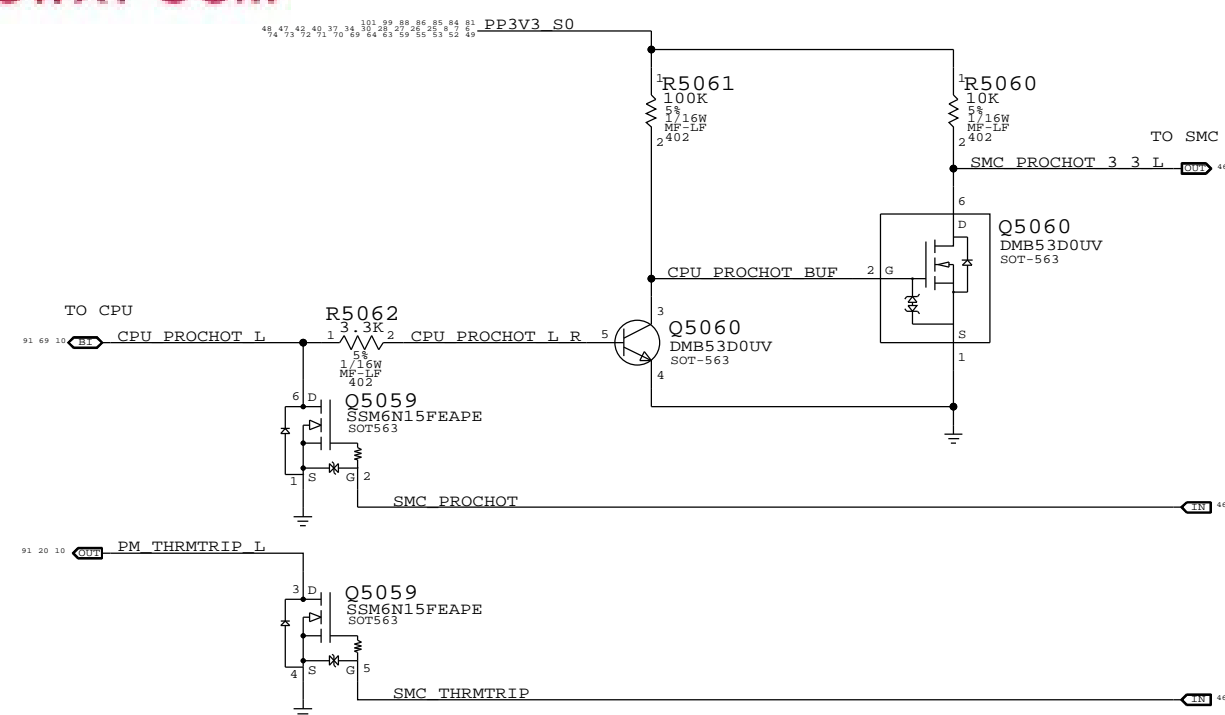
System (Sleep) LED Circuit



CPU PM_EXTTS_L / MEM_EVENT_L Level Shifting

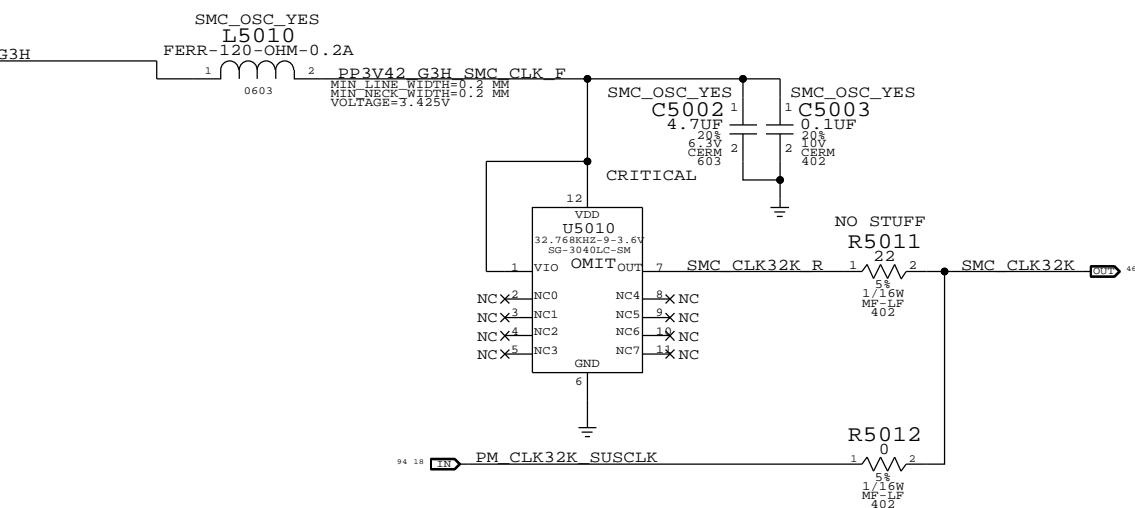


SMC FSB to 3.3V Level Shifting



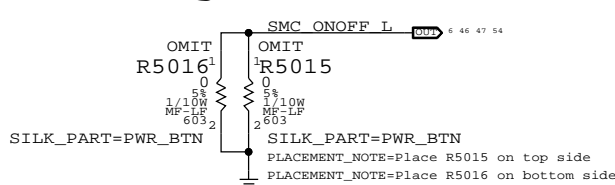
SMC G3Hot 32kHz Oscillator

To support timed wake-up events in G3Hot



SMC ONOFF L	R5070	10K	1	2	5%	1/16W MF-LF 402
G3 POWERON L	R5072	10K	1	2	5%	1/16W MF-LF 402
SMC LID	R5071	100K	1	2	5%	1/16W MF-LF 402
SMC TX L	R5073	10K	1	2	5%	1/16W MF-LF 402
SMC RX L	R5074	100K	1	2	5%	1/16W MF-LF 402
SYS ONEWIRE NO STUFF	R5075	2.0K	1	2	5%	1/16W MF-LF 402
SMC TMS	R5077	10K	1	2	5%	1/16W MF-LF 402
SMC TDO	R5078	10K	1	2	5%	1/16W MF-LF 402
SMC TDI	R5079	10K	1	2	5%	1/16W MF-LF 402
SMC TCK	R5080	10K	1	2	5%	1/16W MF-LF 402
SMC BIL BUTTON L	R5081	10K	1	2	5%	1/16W MF-LF 402
SMC BC ACOK	R5087	470K	1	2	5%	1/16W MF-LF 402
SMS INT L	R5093	10K	1	2	5%	1/16W MF-LF 402
SMC BATT ULP L	R5096	100K	1	2	5%	1/16W MF-LF 402
SMC PA0	R5091	100K	1	2	5%	1/16W MF-LF 402
SMC EXCARD OC L	R5092	100K	1	2	5%	1/16W MF-LF 402
SMC ADAPTER EN	R5085	10K	1	2	5%	1/16W MF-LF 402
SMC CASE OPEN	R5086	10K	1	2	5%	1/16W MF-LF 402
SMC EXCARD CP	R5088	10K	1	2	5%	1/16W MF-LF 402
PM SLP S5 L	R5090	100K	1	2	5%	1/16W MF-LF 402
PM SLP S4 L	R5094	100K	1	2	5%	1/16W MF-LF 402

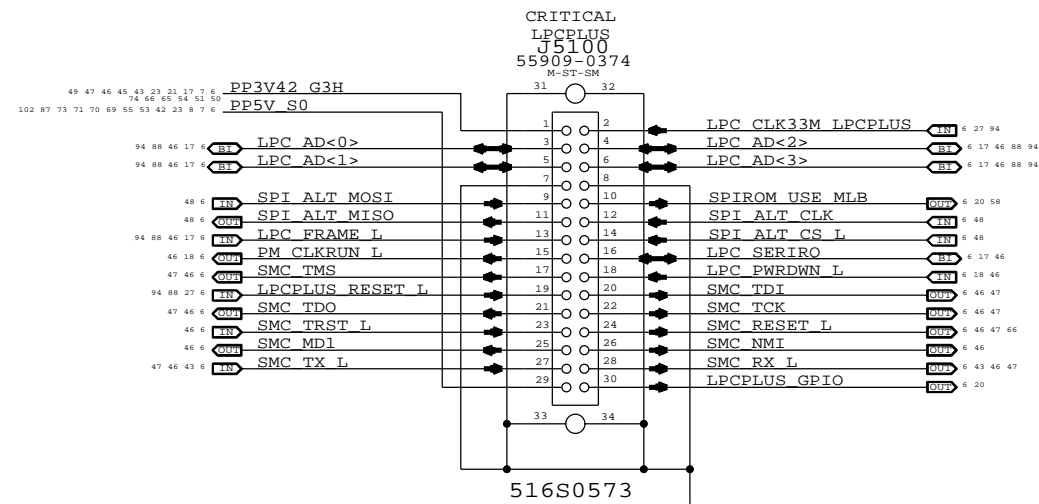
Debug Power "Buttons"



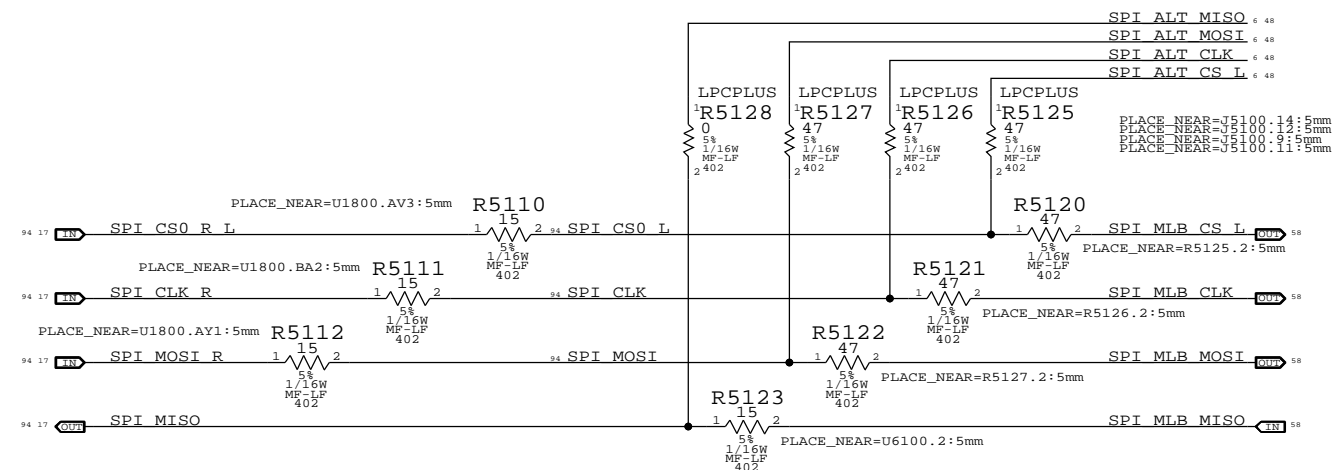
SYNC MASTER=K17 REF	SYNC DATE=06/17/2009
PAGE TITLE	
SMC Support	
Apple Inc.	DRAWING NUMBER
REVISION	SIZE
BRANCH	D
PAGE	50 OF 132
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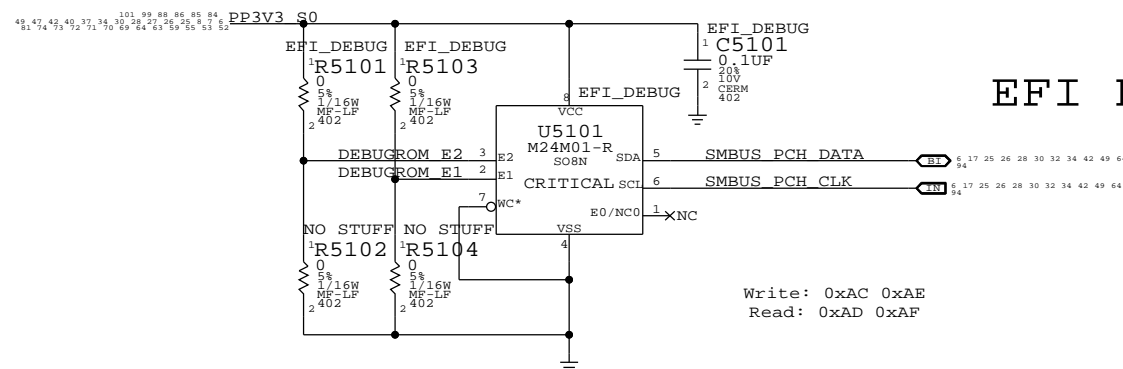
LPC+SPI Connector




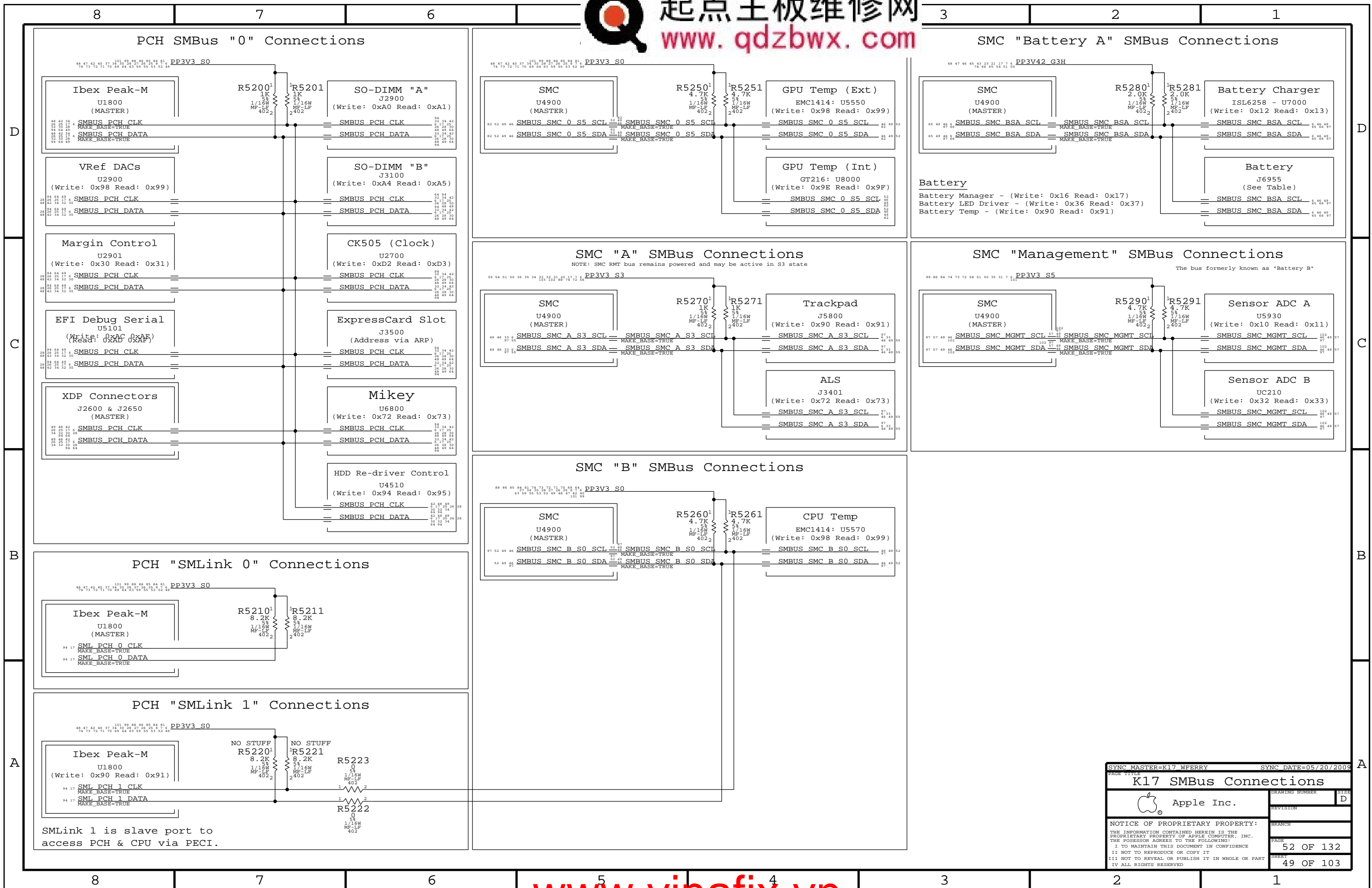
SPI Bus Series Termination

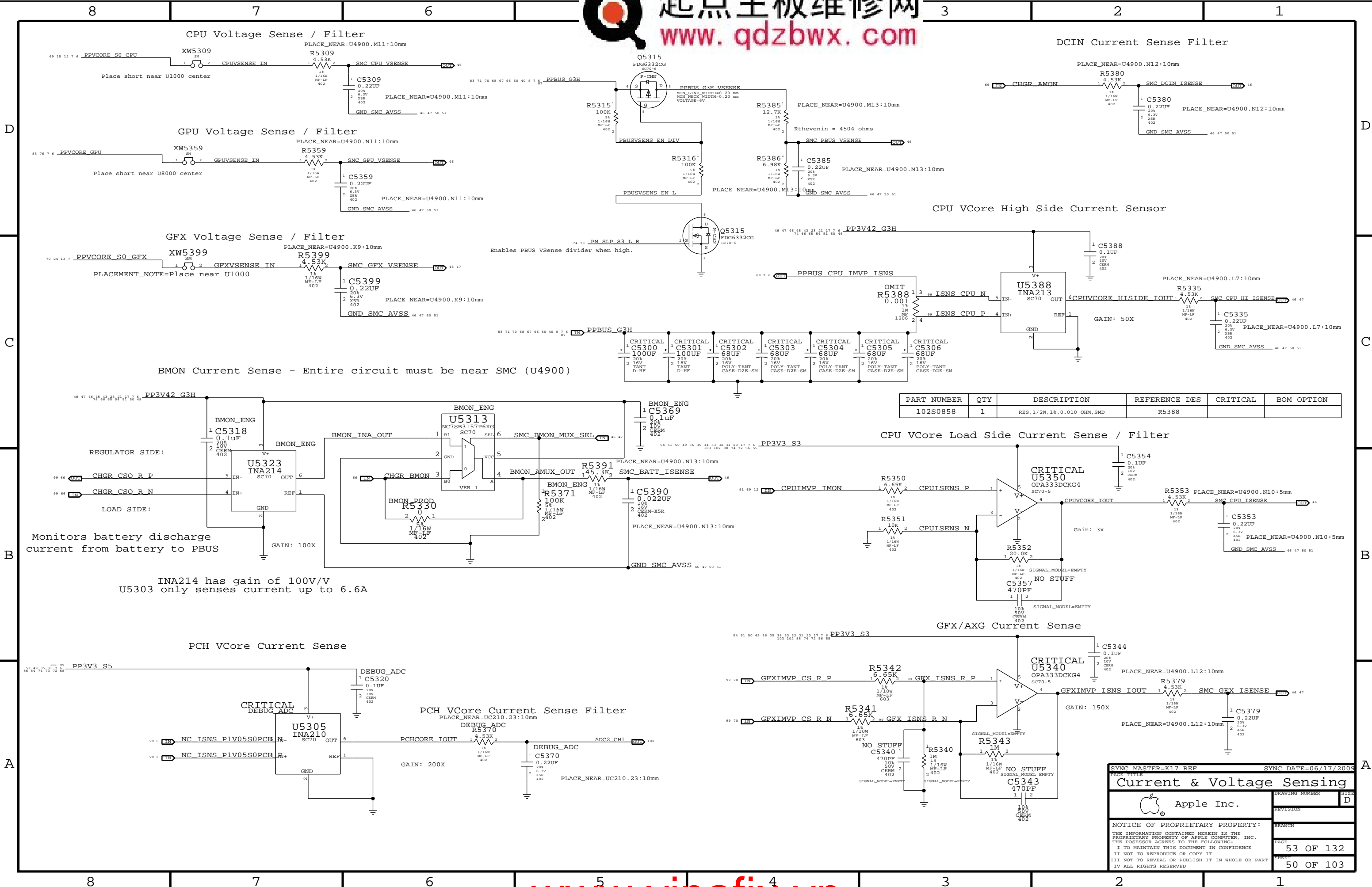


EFI Debug ROM



SYNC_MASTER=T22_MLB		SYNC_DATE=03/30/2009	
PAGE 11111			
LPC+SPI Debug Connector			
 Apple Inc.		DRAWING NUMBER	SIZE
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
102S0858	1	RES,1/2W,1%,0.010 OHM,SMD	R5388		

Monitors battery discharge current from battery to PBUS

INA214 has gain of 100V/V
U5303 only senses current up to 6.6A

SYNC MASTER=K17 REF

SYNC DATE=06/17/2009

Current & Voltage Sensing

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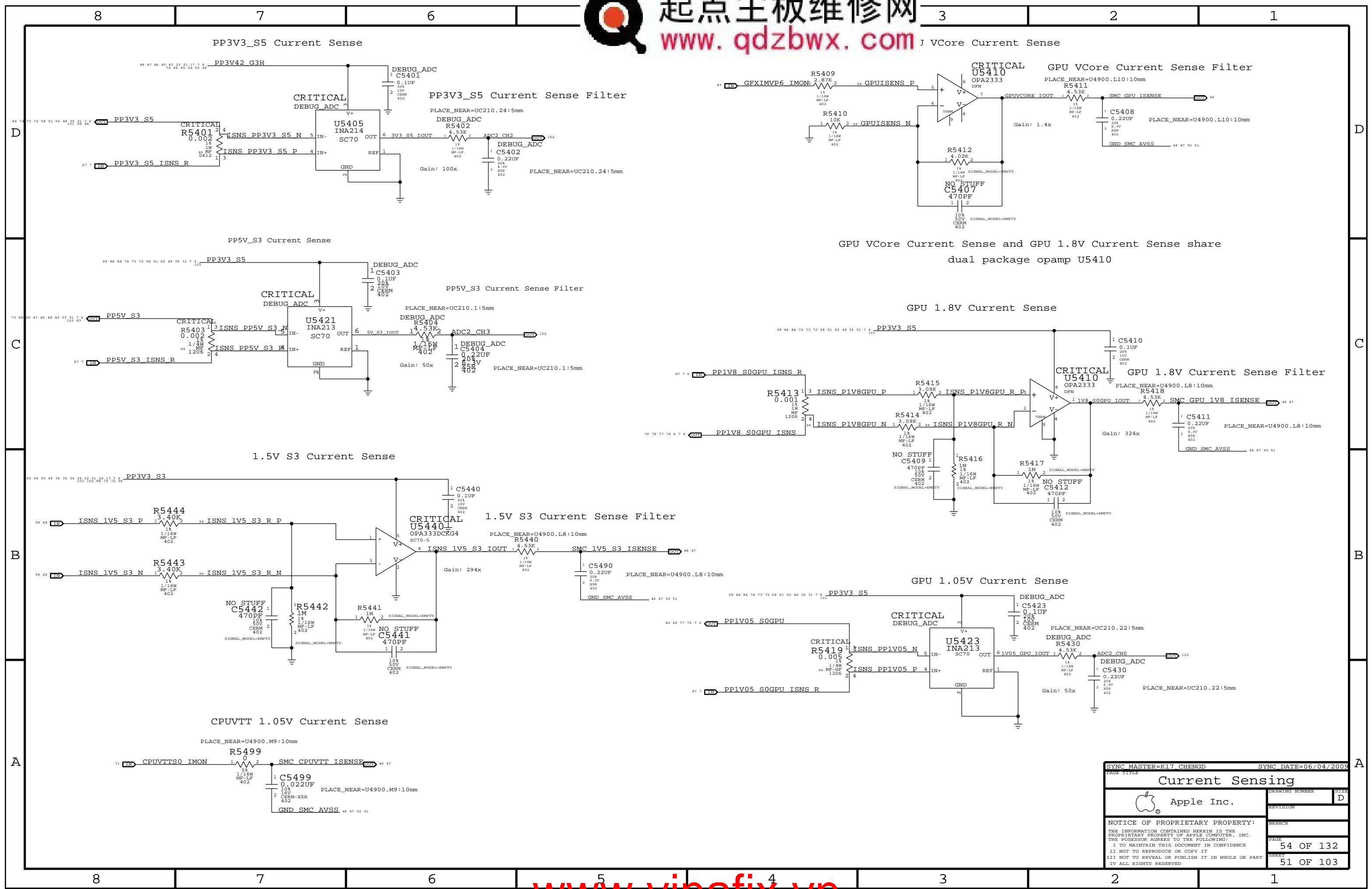
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PAGE

SHEET

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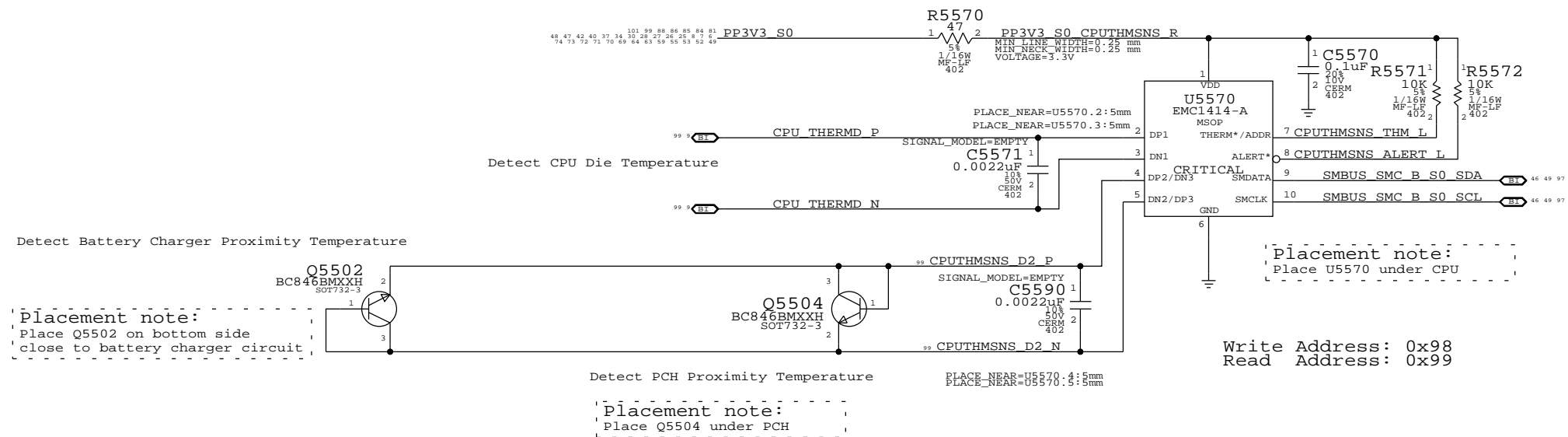
50 OF 103



SYNC MASTER=K17 CHENG D		SYNC DATE=06/04/2009	
PAGE TITLE		Current Sensing	
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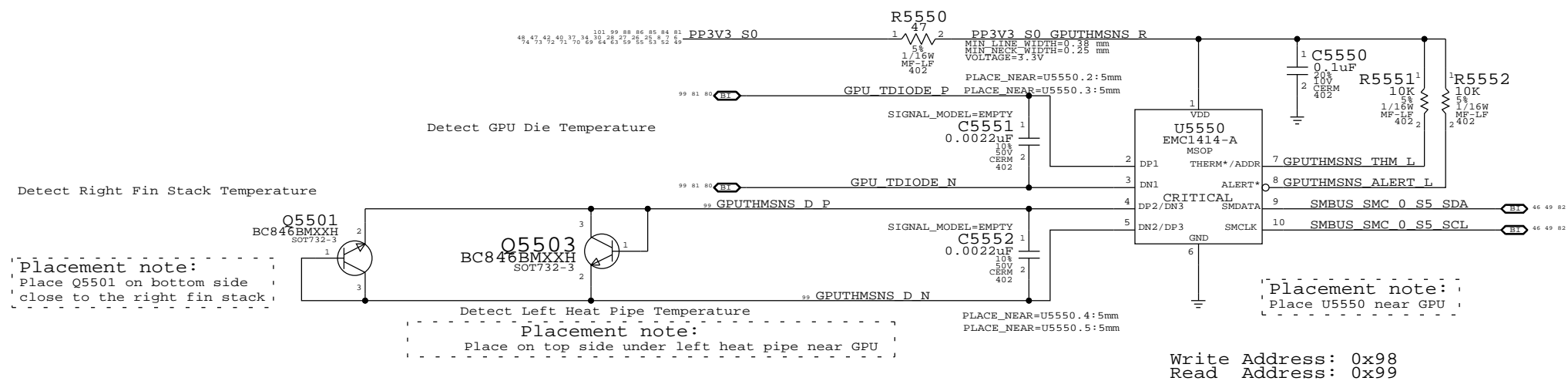


CPU Proximity/CPU Die/PCH Proximity/Battery Charger Proximity



Note: EMC1414 can perform Beta Compensation for External Diode 1 only

GPU Proximity/GPU Die/Left Heat Pipe/Right Fin Stack



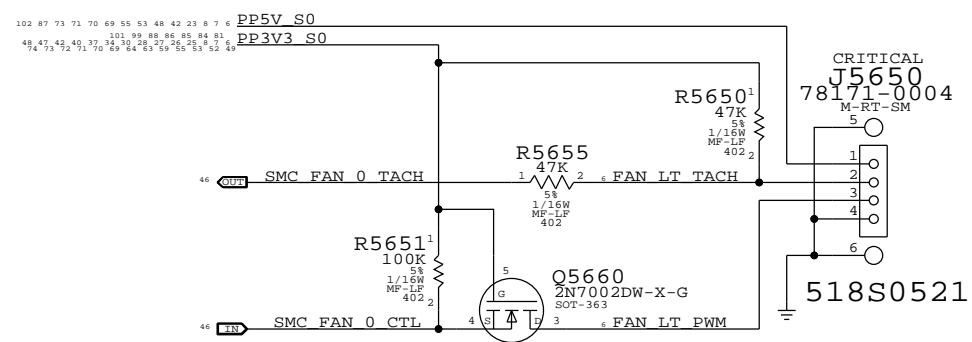
SYNC MASTER=K17_CHENGDD		SYNC DATE=07/08/2009	
PAGE TITLE		Thermal Sensors	
Apple Inc.		DRAWING NUMBER	SIZE
		REVISION	D
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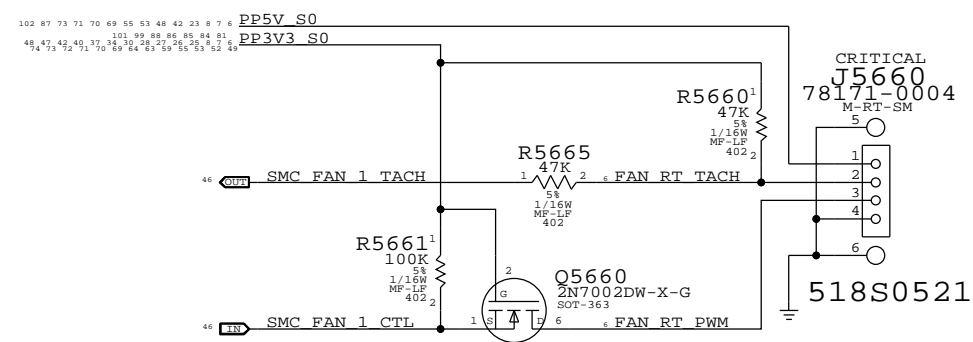
D
C
B
A

D
C
B
A

Left Fan



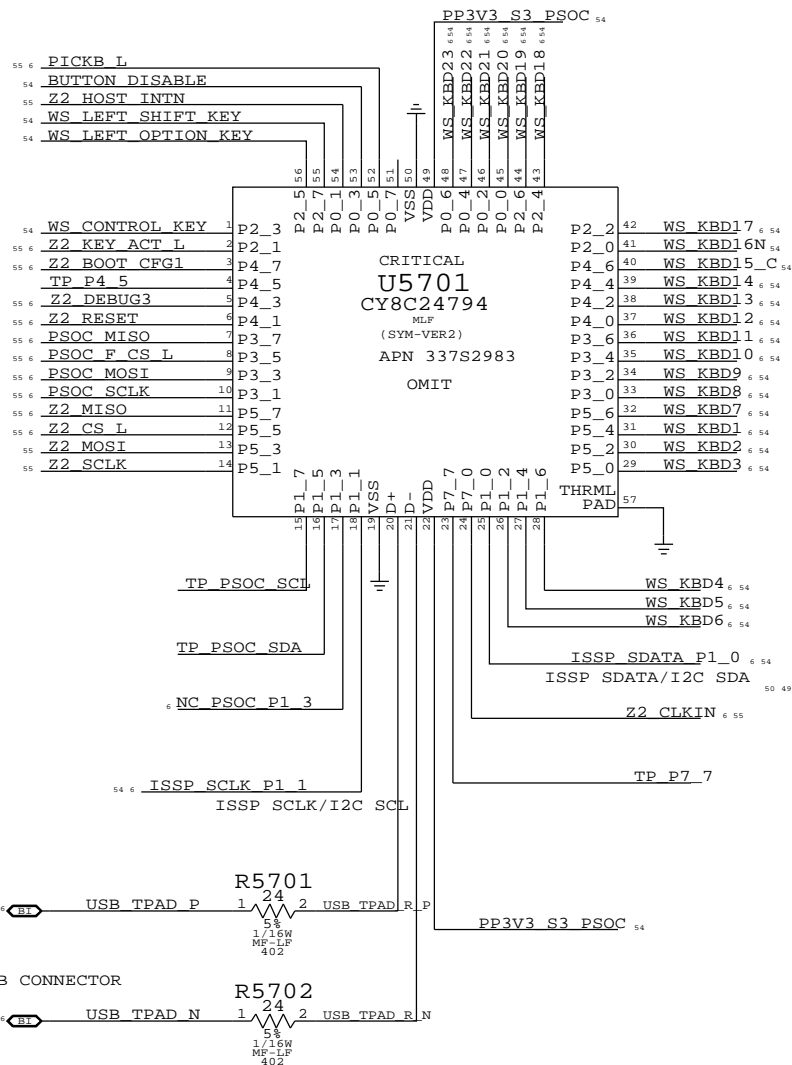
Right Fan





PSOC USB CONTROLLER

USB INTERFACES TO MLBACKPAD PICK BUTTONS
SPI HOST TO Z2
KEYBOARD SCANNER



U5701 CHIP DECOUPLING

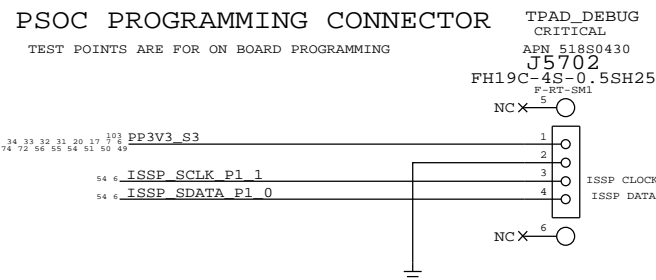
PLACE C5701, C5702 & C5703
CLOSE TO U5701VDD PIN 22

PLACE C5704, C5705 & C5706
CLOSE TO U5701VDD PIN 49

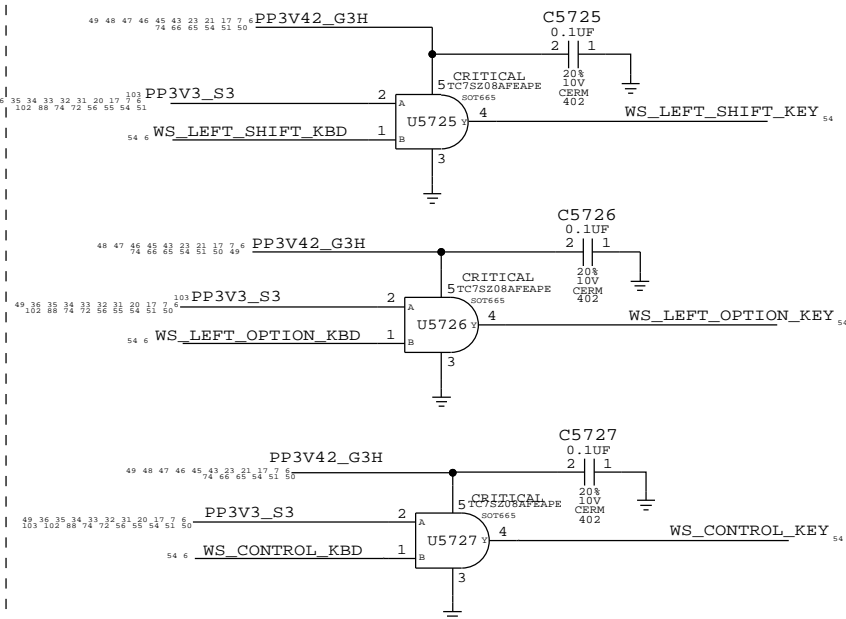
IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	100UA	2.55 KOHM	0.0255 V	0.255E-6 W
3V3 LDO	VDD	80UA	10 OHM	0.204 V	16.32E-6 W
PSOC	VOUT	60MA MAX	0.2 OHM	0.6 V	36E-3 W
	VDD	60MA MAX	0.2 OHM	0.012 V	0.72E-3 W
	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
	VDD	14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

PSOC PROGRAMMING CONNECTOR

TEST POINTS ARE FOR ON BOARD PROGRAMMING

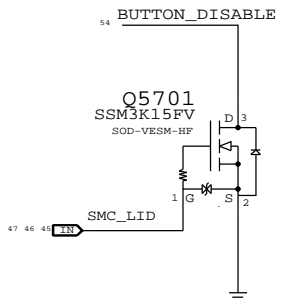


ISOLATION CIRCUIT



TPAD BUTTONS DISABLE

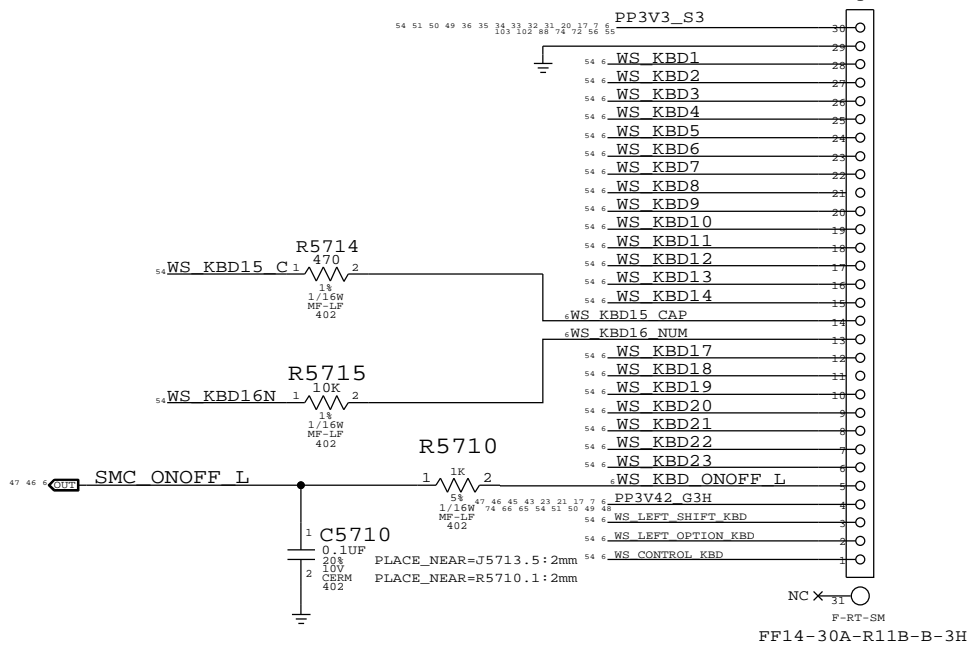
PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB



THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

KEYBOARD CONNECTOR

J5713
APN 518S0637
NC X-32

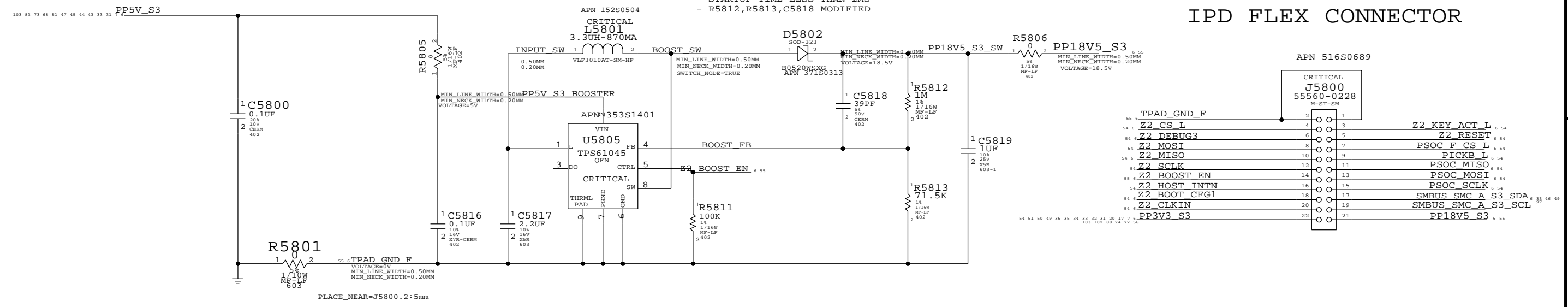




BOOSTER + L5801 FOR SENSORS

- BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
 - DROOP LINE REGULATION
 - RIPPLE TO MEET ERS
 - 100-300 KHZ CLEAN SPECTRUM
 - STARTUP TIME LESS THAN 2MS
 - R5812,R5813,C5818 MODIFIED

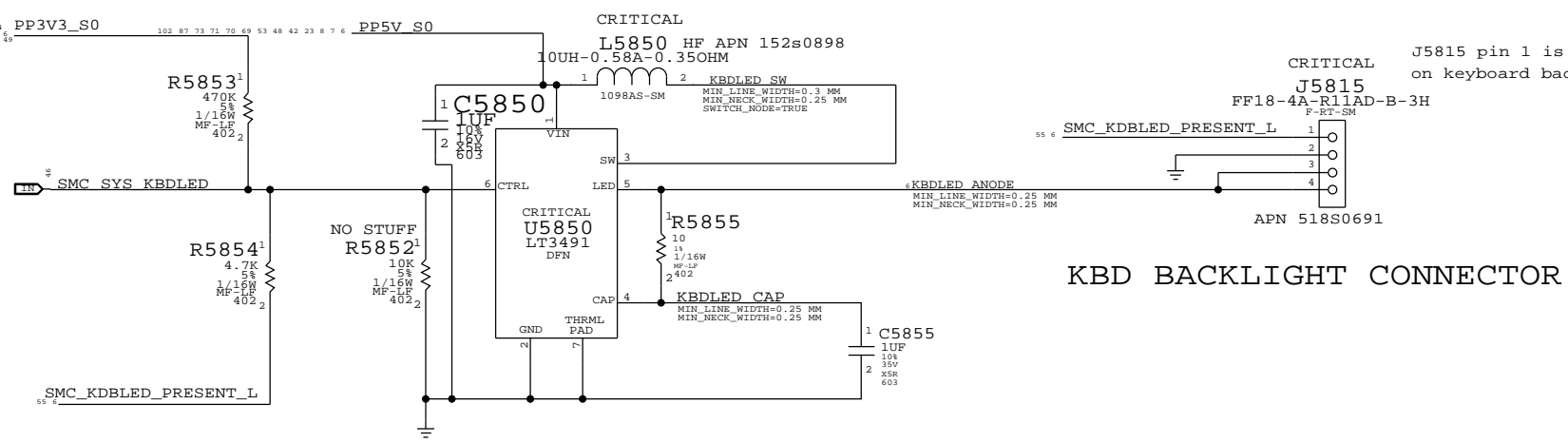
IPD FLEX CONNECTOR




Keyboard LED Driver

To detect Keyboard backlight, SMC will tristate SMC_SYS_KBDLED:
LOW = keyboard backlight present
HIGH= keyboard backlight not present
BOM OPTION: KBDLED_YES

R5853 ALWAYS PRESENT

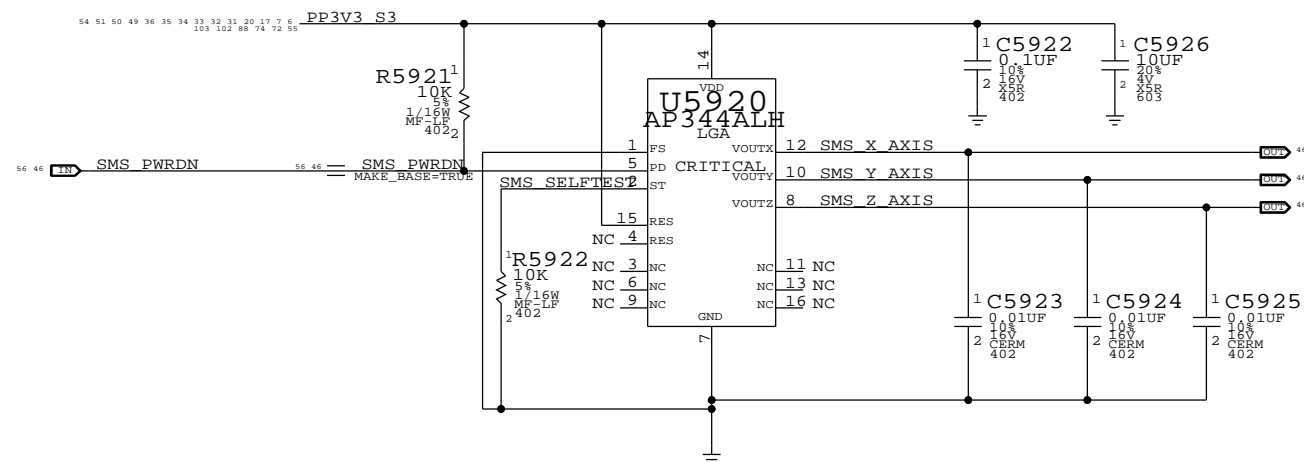


SYNC MASTER=K17 WFERRY		SYNC DATE=06/09/2009	
PAGE TITLE			
WELLSPRING 2		DRAWING NUMBER	SIZE
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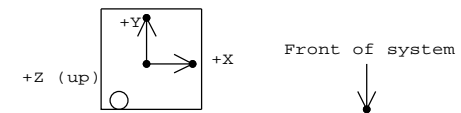


Analog SMS


R5921 PULLS UP SMS_PWRDN TO TURN OFF SMS WHEN PIN IS NOT BEING DRIVEN BY SMC



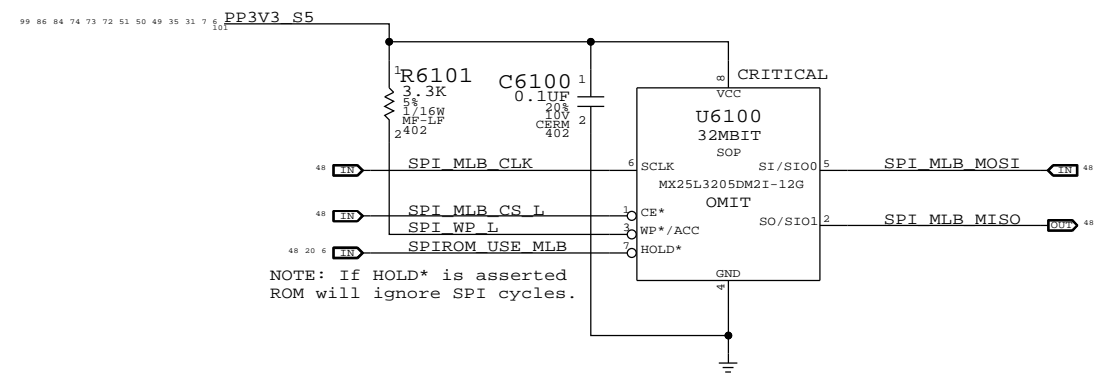
Desired orientation when placed on board top-side:

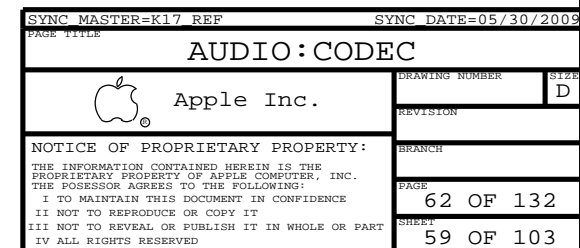
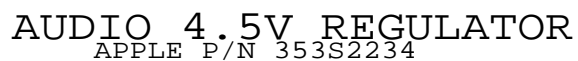


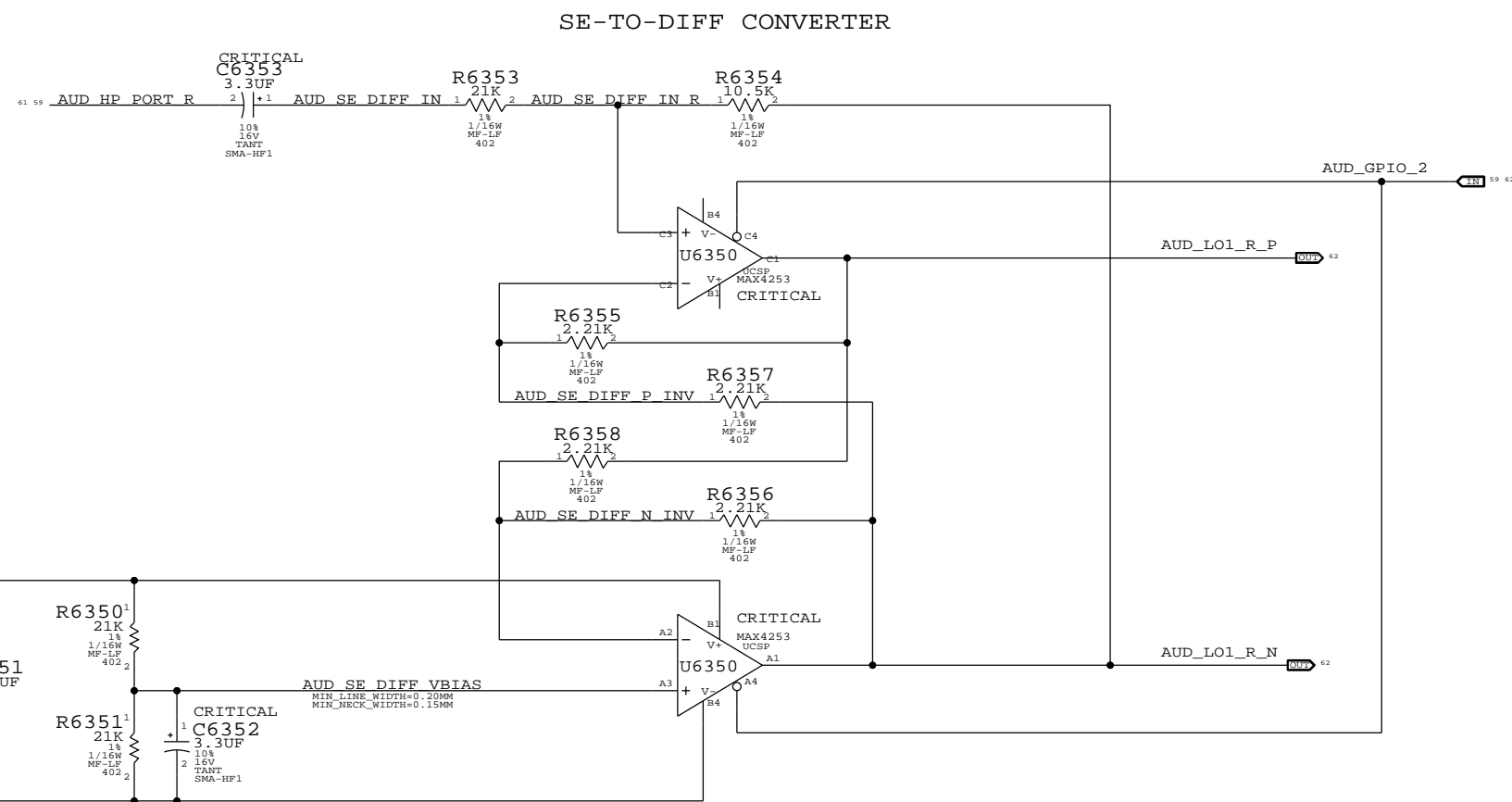
Circle indicates pin 1 location when placed in correct orientation


SYNC_MASTER=K20A_MLB		SYNC_DATE=03/26/2009	
PAGE TITLE			
Sudden Motion Sensor (SMS)			
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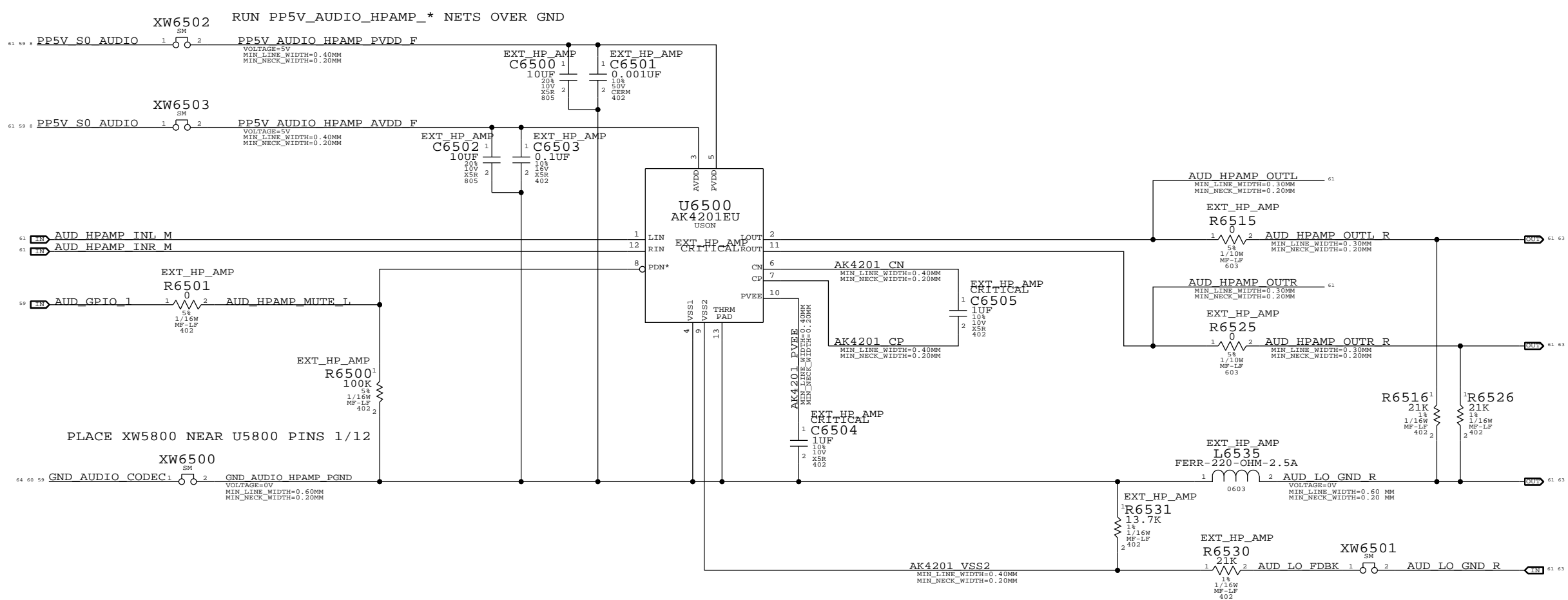
SYNC MASTER-K17 REF		SYNC DATE=05/30/2009	
PAGE TITLE			
AUDIO: LINE IN			
 Apple Inc.		DRAWING NUMBER	
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		REVISION	
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		PAGE	
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		60 OF 103	



HEADPHONE

APN: 353S2347
VOLTAGE GAIN: 1.53

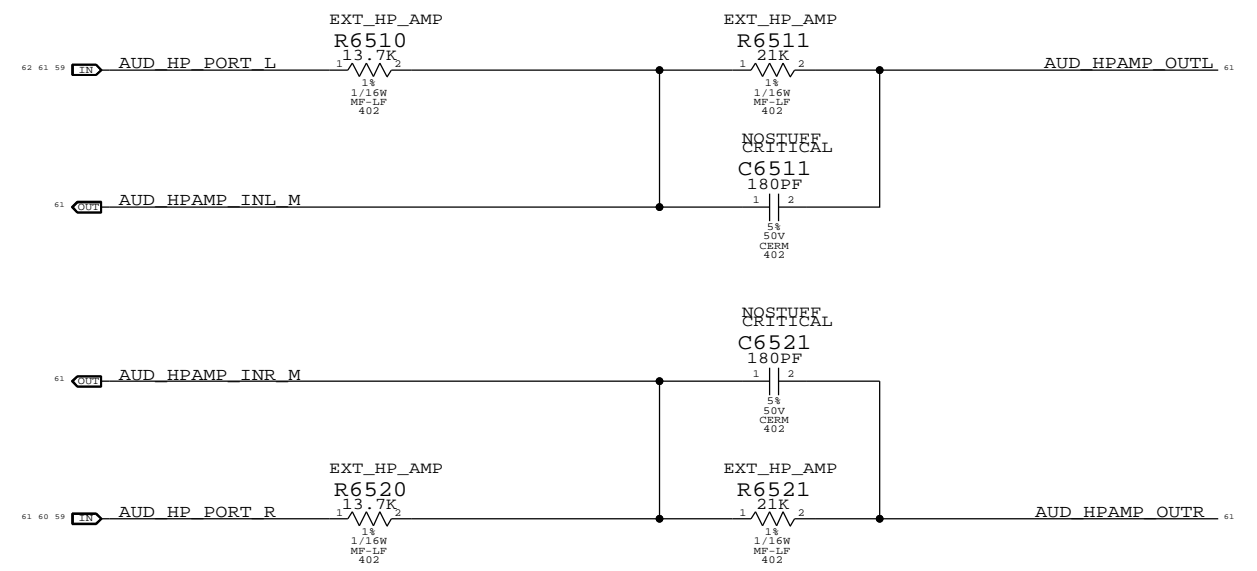
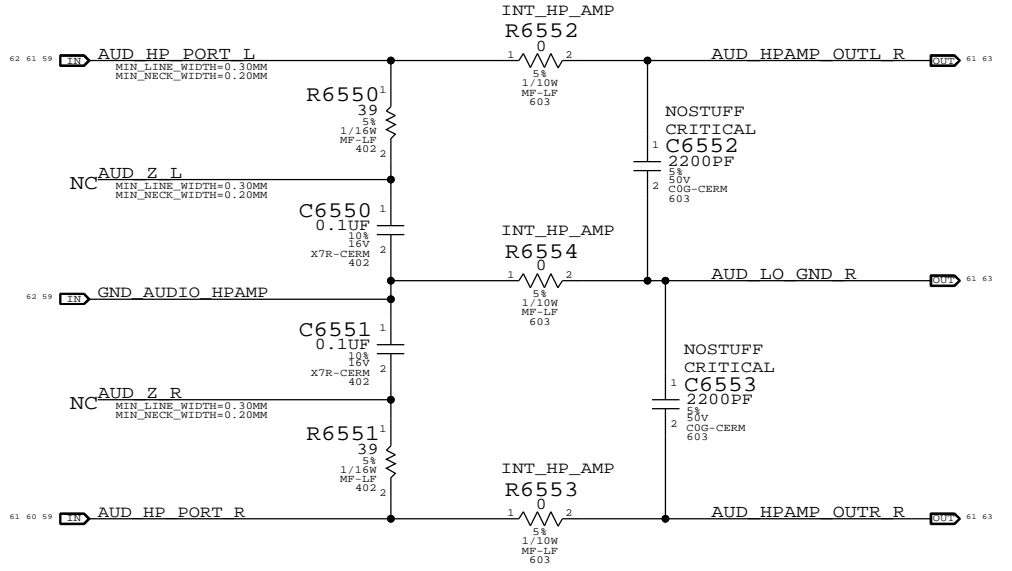
PLACE XW5802 & XW5803 NEAR PP5V_S0_AUDIO




PLACE XW5800 NEAR U5800 PINS 1/12

CS4206A HP OUT ZOBEL NETWORK &
1ST ORDER DAC FILTER PLACEHOLDER

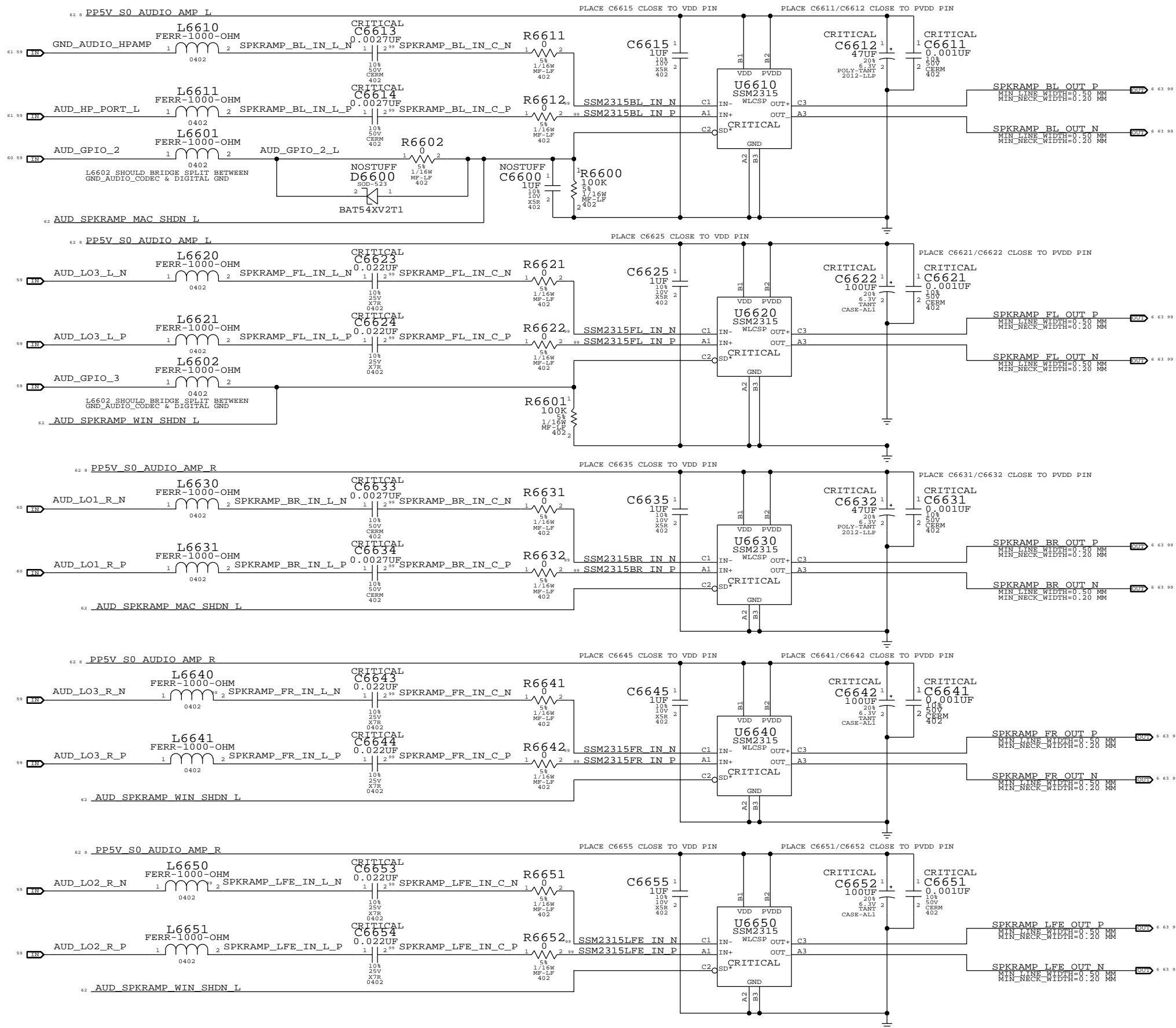
1ST ORDER DAC FILTER
LP: 42.10 KHZ




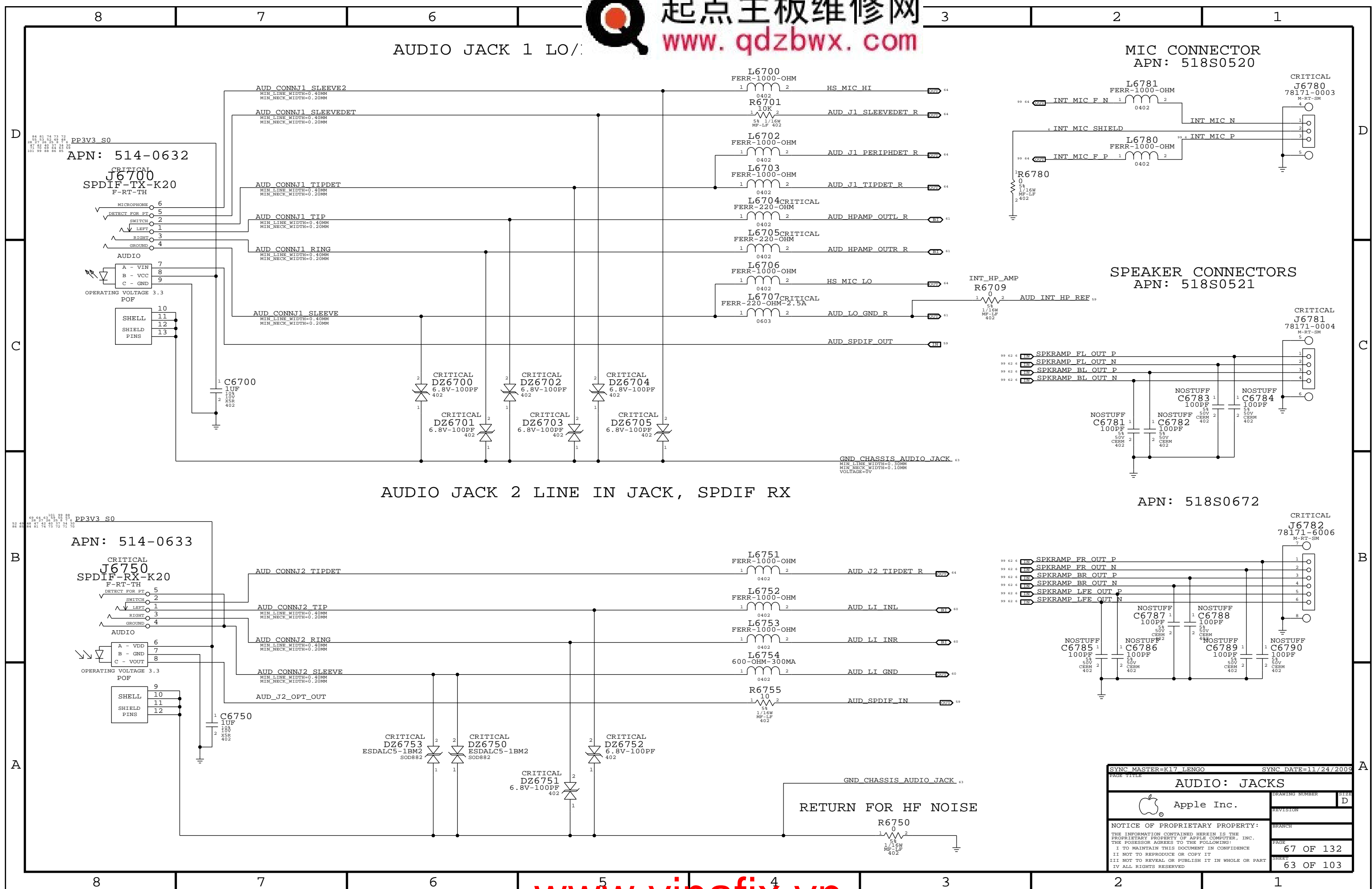
SYNC MASTER=K17 REF		SYNC DATE=05/30/2009	
PAGE TITLE			
AUDIO: HEADPHONE OUT			
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5X MONO SPEAKER AMPLIFIERS ()
APN: 353S2500
GAIN = +6 DB
FC (SPEAKERS BL/BR) = ~737 HZ
FC (SPEAKERS FL/FR/LFE) = ~90 HZ

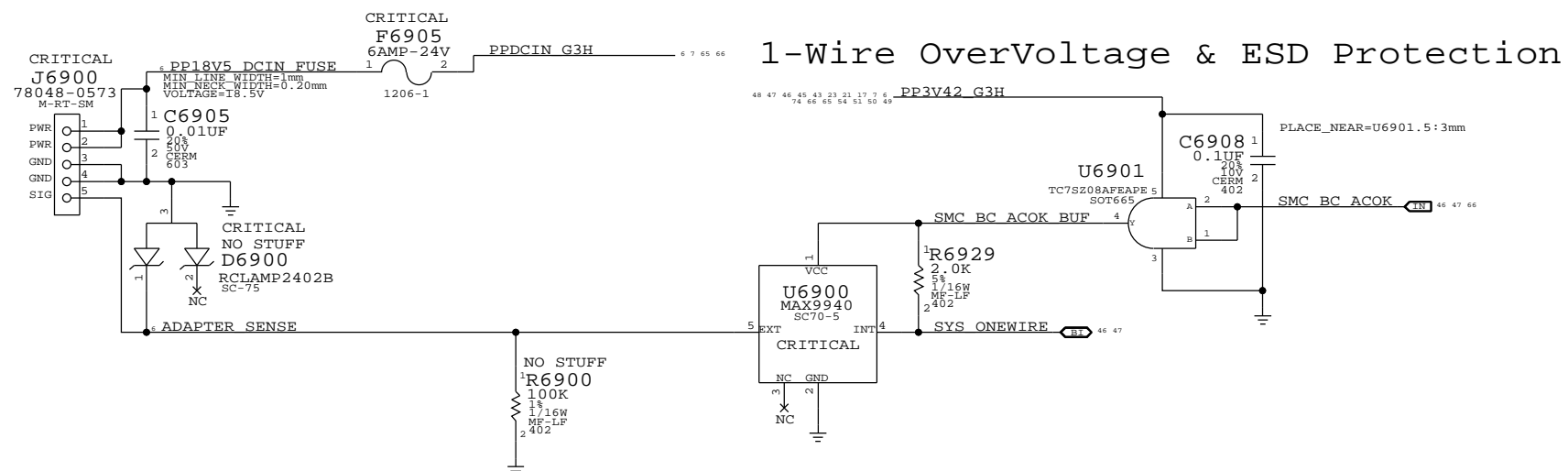


SYNC MASTER=K17 REF		SYNC DATE=05/30/2009	
PAGE TITLE			
AUDIO:SPEAKER AMP			
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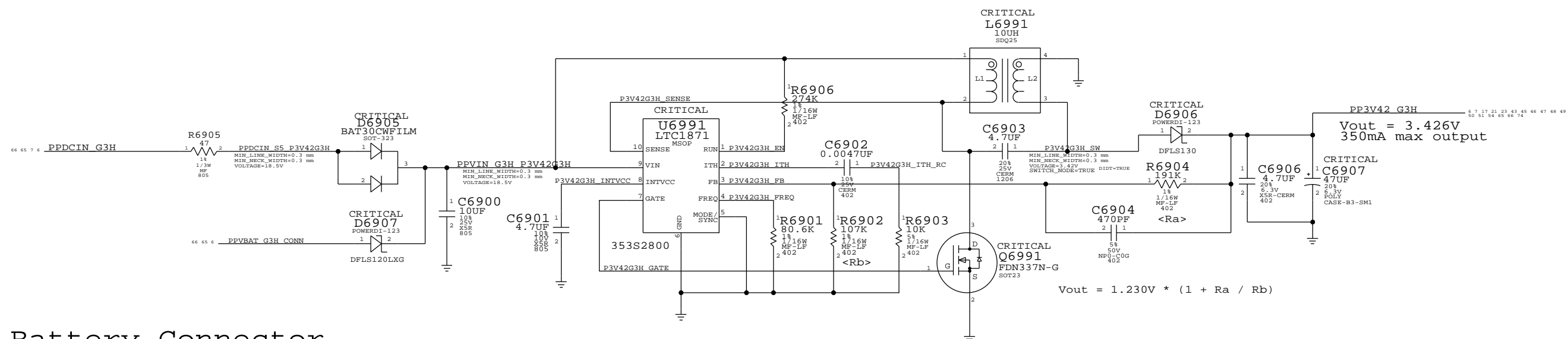


MagSafe DC Power Jack

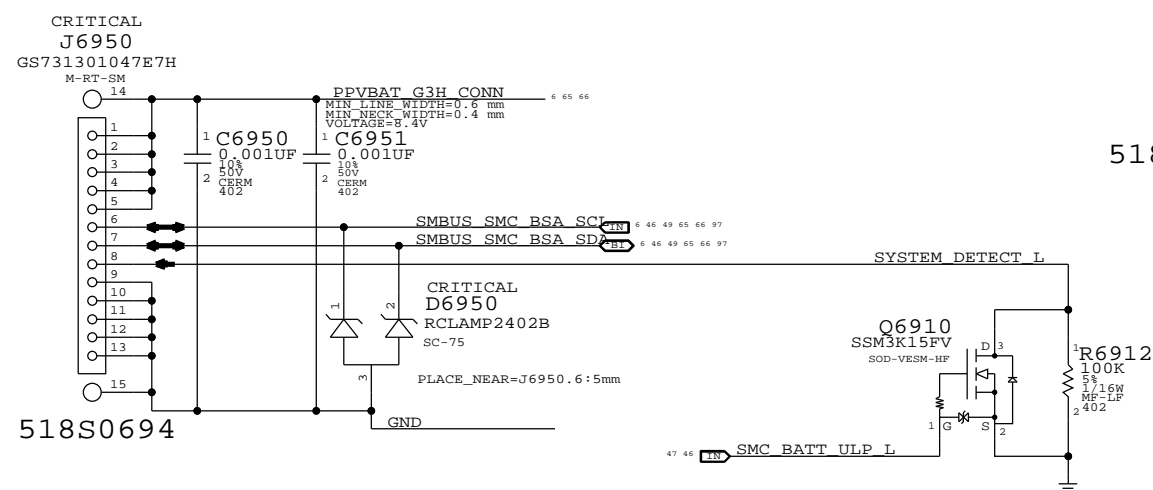


3.425V "G3Hot" Supply

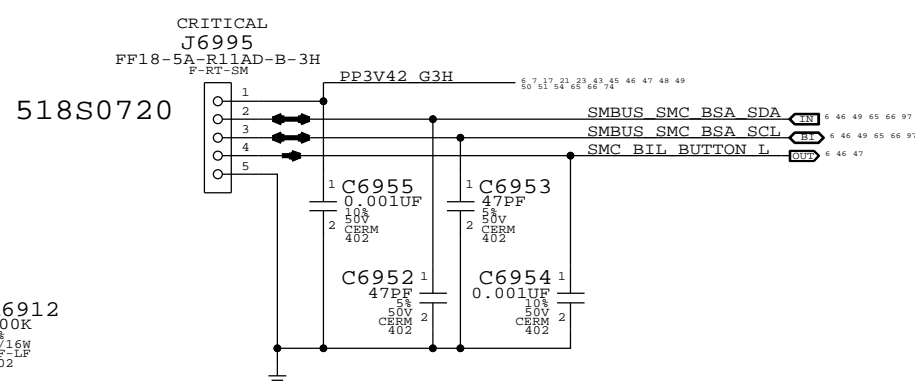
Supply needs to guarantee 3.31V delivered to SMC VRef generator




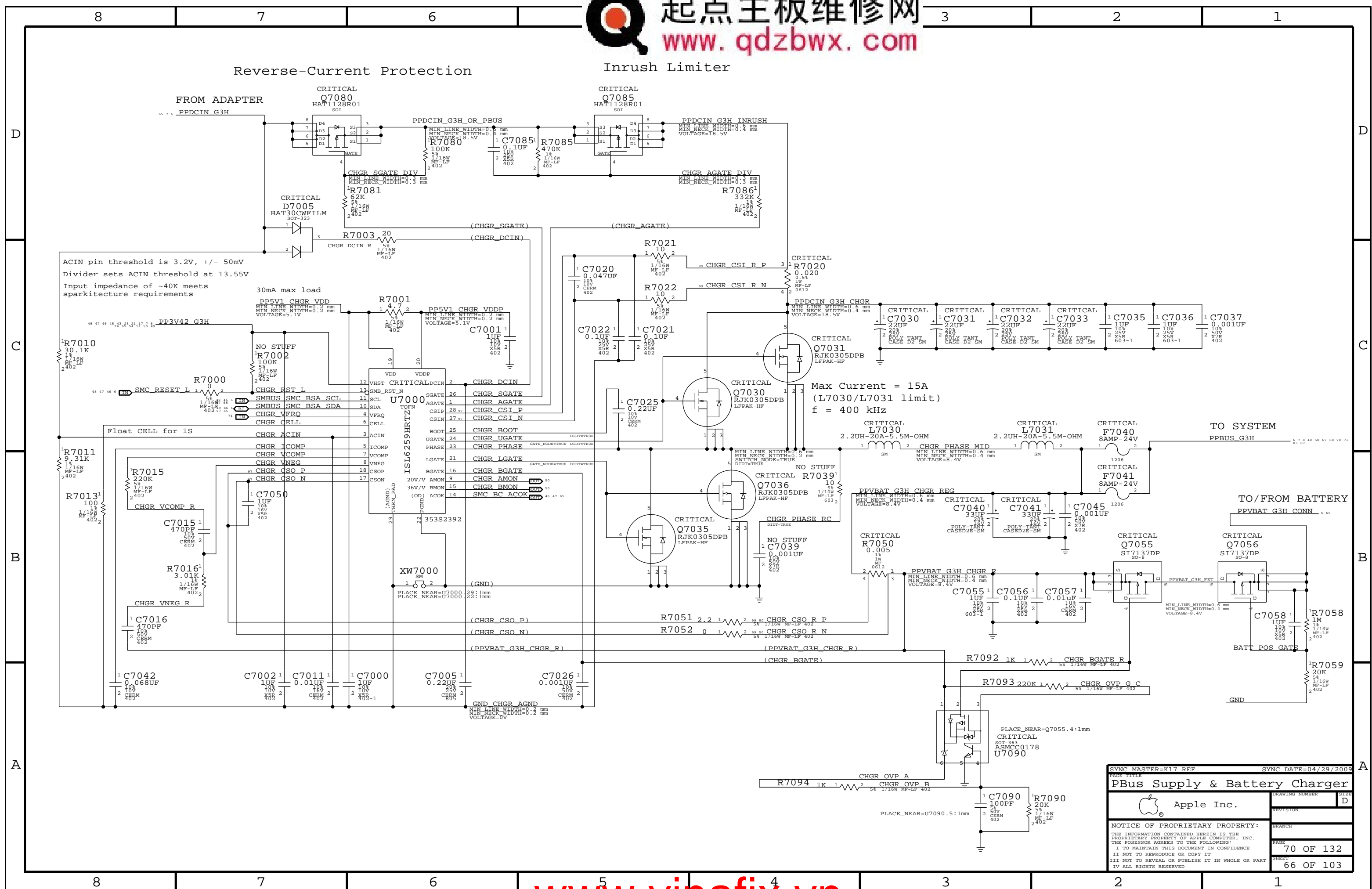
Battery Connector

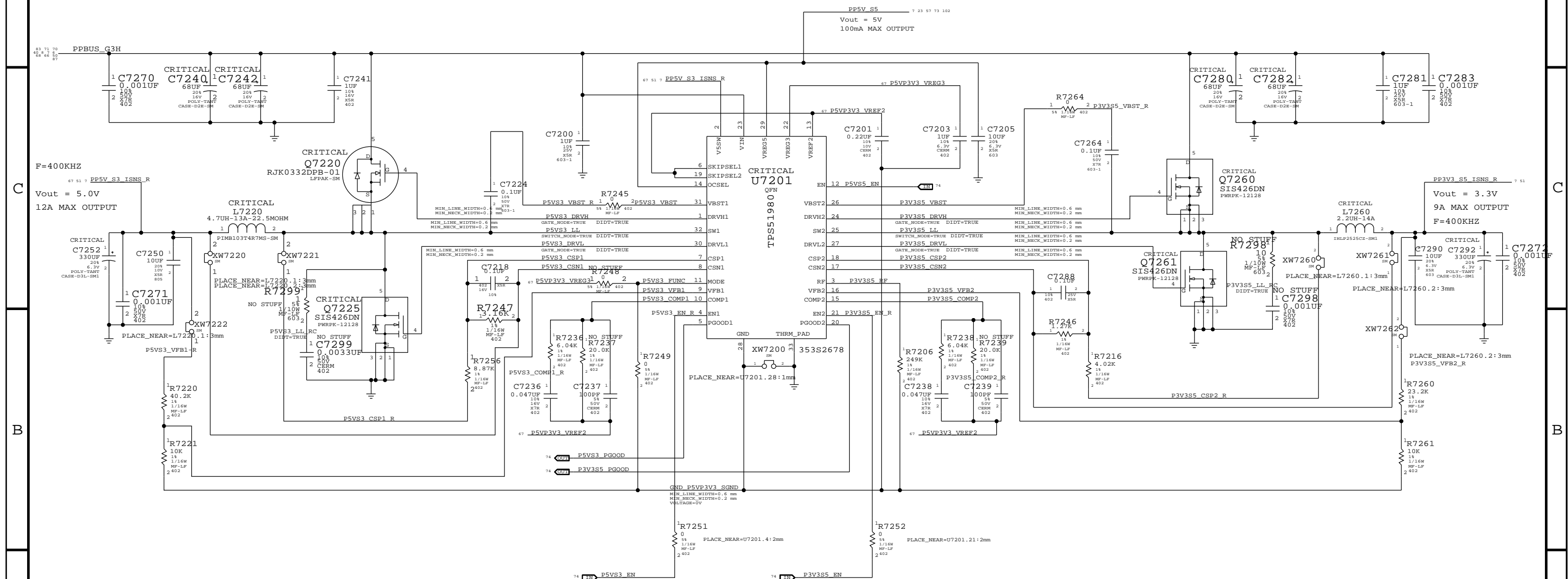



BIL Connector

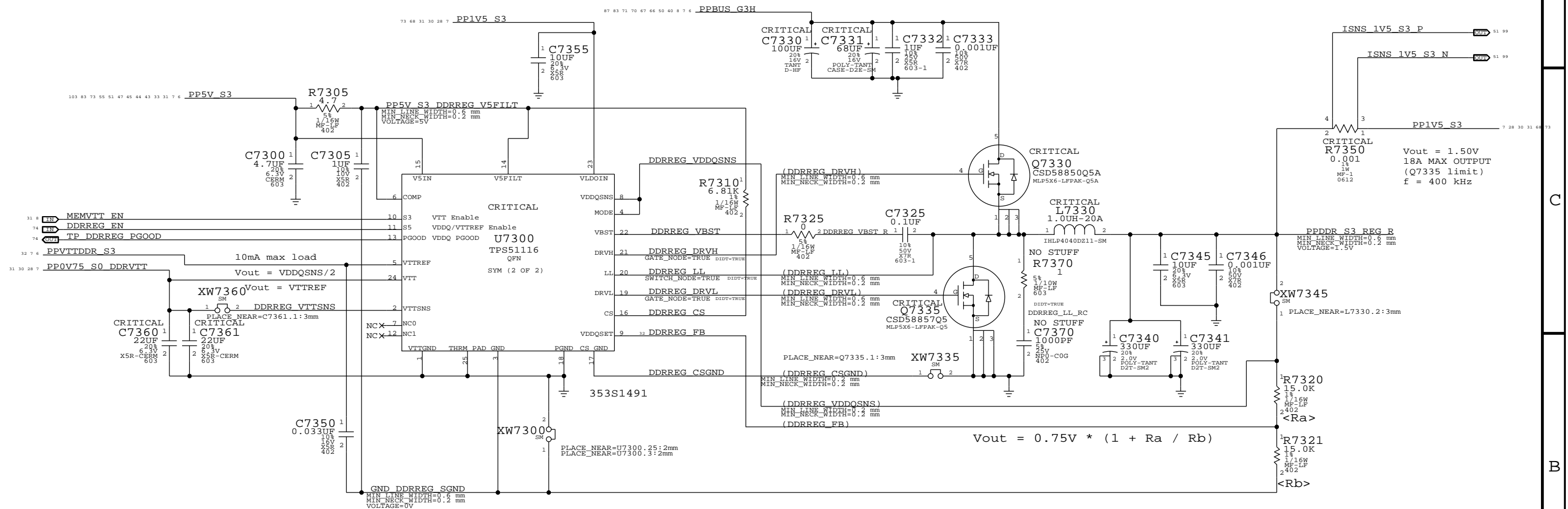



SYNCH MASTER=K17 REF		SYNCH DATE=04/29/2009	
PAGE 1 OF 1			
DC-In & Battery Connectors			
 Apple Inc.		DRAWING NUMBER REVISION	
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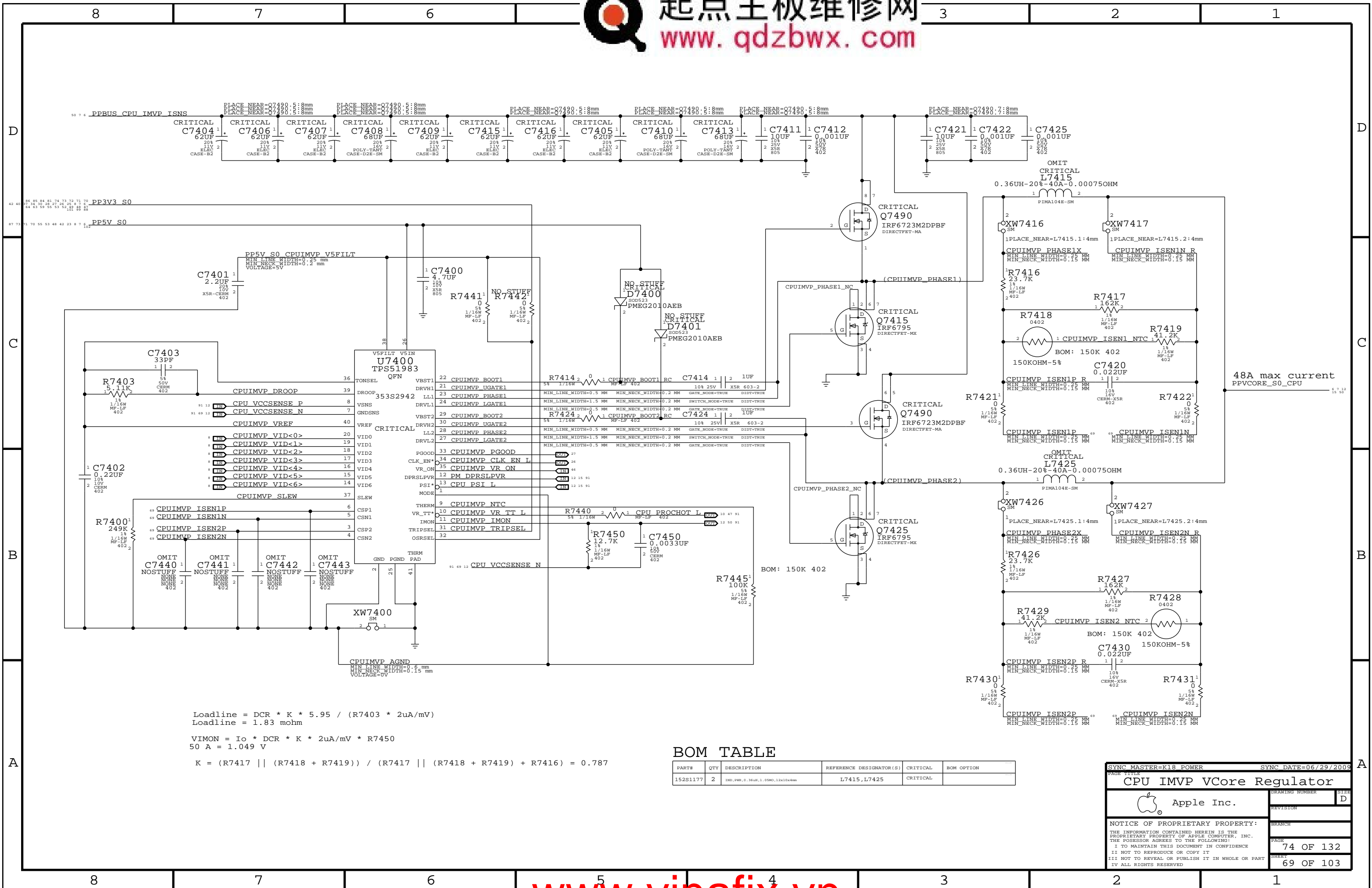




SYNC MASTER-K20A MLB		SYNC DATE=03/26/2009	
PAGE TITLE			
5V / 3.3V Power Supply			
 Apple Inc.		DRAWING NUMBER	SIZE
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PAGE TITLE			
1.5V DDR3 Supply			
 Apple Inc.		DRAWING NUMBER	SIZE
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Loadline = DCR * K * 5.95 / (R7403 * 2uA/mV)
Loadline = 1.83 mohm

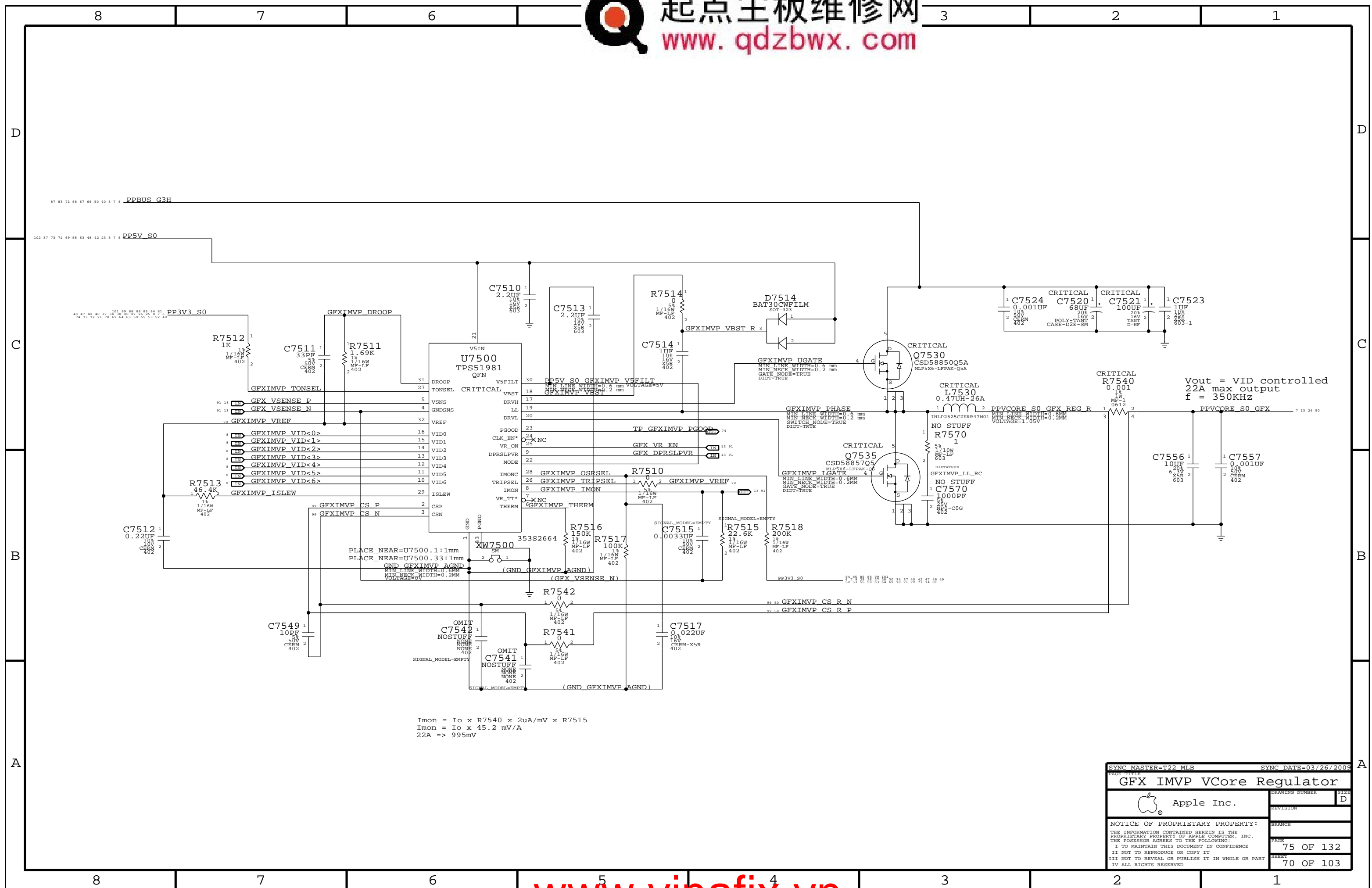
VIMON = Io * DCR * K * 2uA/mV * R7450
50 A = 1.049 V

K = (R7417 || (R7418 + R7419)) / (R7417 || (R7418 + R7419) + R7416) = 0.787

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S1177	2	IND, PWR, 0.36uH, 1.05MO, 12x10x4mm	L7415, L7425	CRITICAL	

SYNC MASTER=K18 POWER		SYNC DATE=06/29/2009	
PAGE TITLE			
CPU IMVP VCore Regulator			
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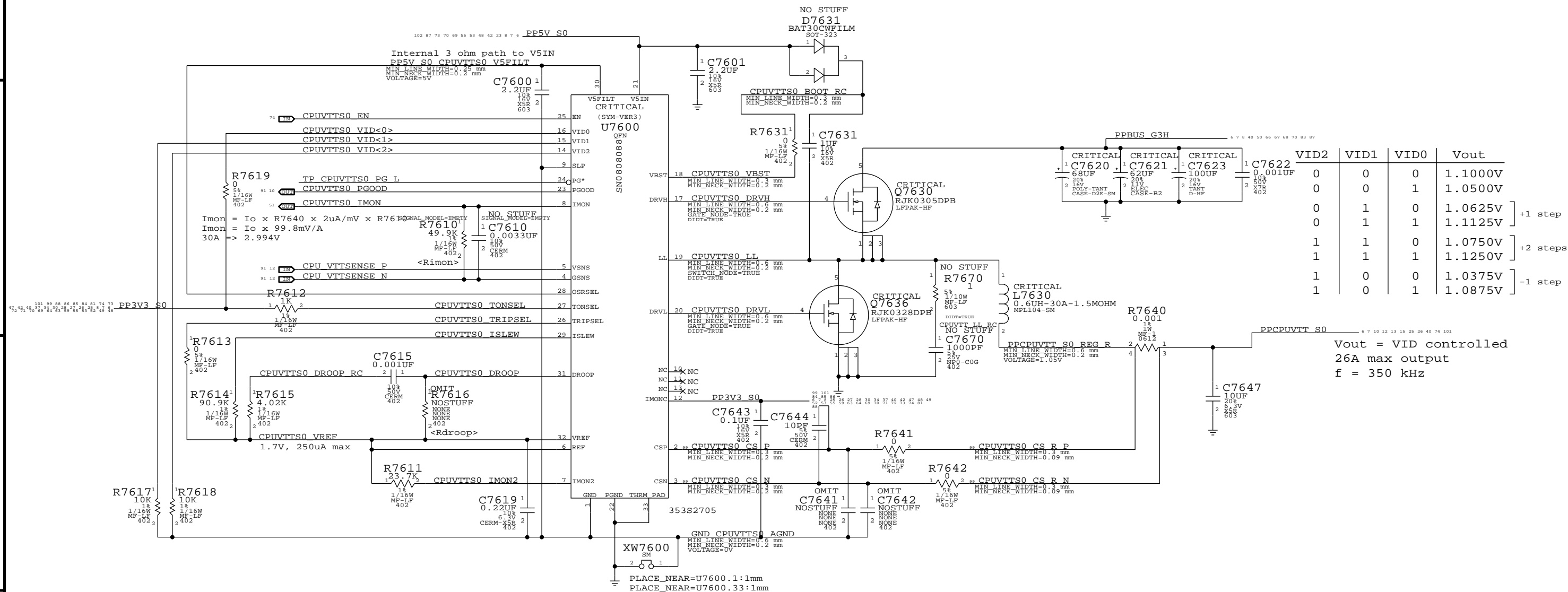


Imon = Io x R7540 x 2uA/mV x R7515
Imon = Io x 45.2 mV/A
22A => 995mV

SYNC MASTER=T22_MLB		SYNC DATE=03/26/2009	
PAGE TITLE		GFX IMVP VCore Regulator	
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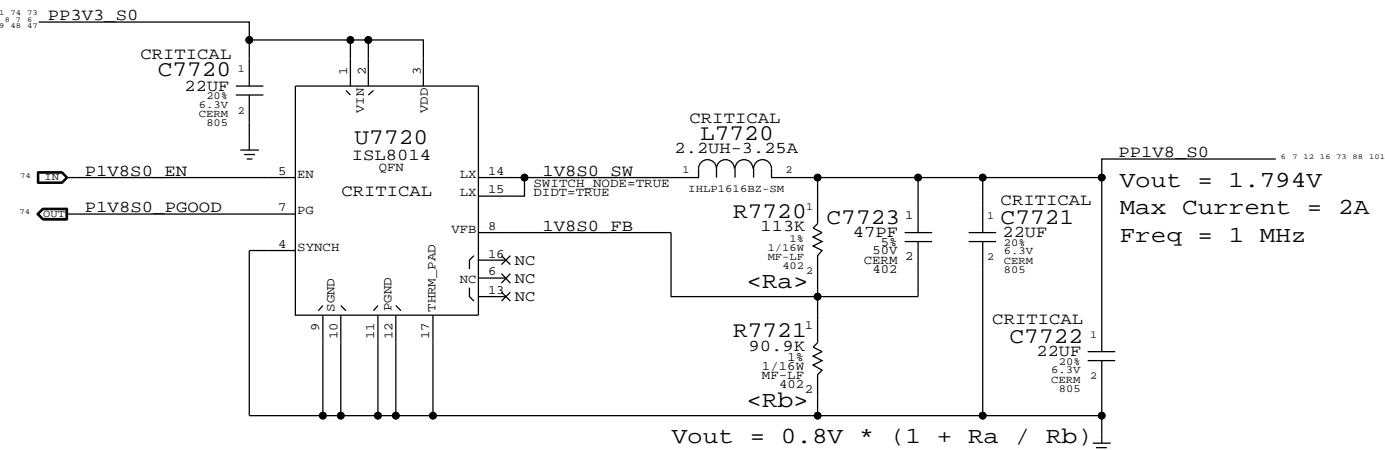


CPU VTT (1.05V S0) Regulator

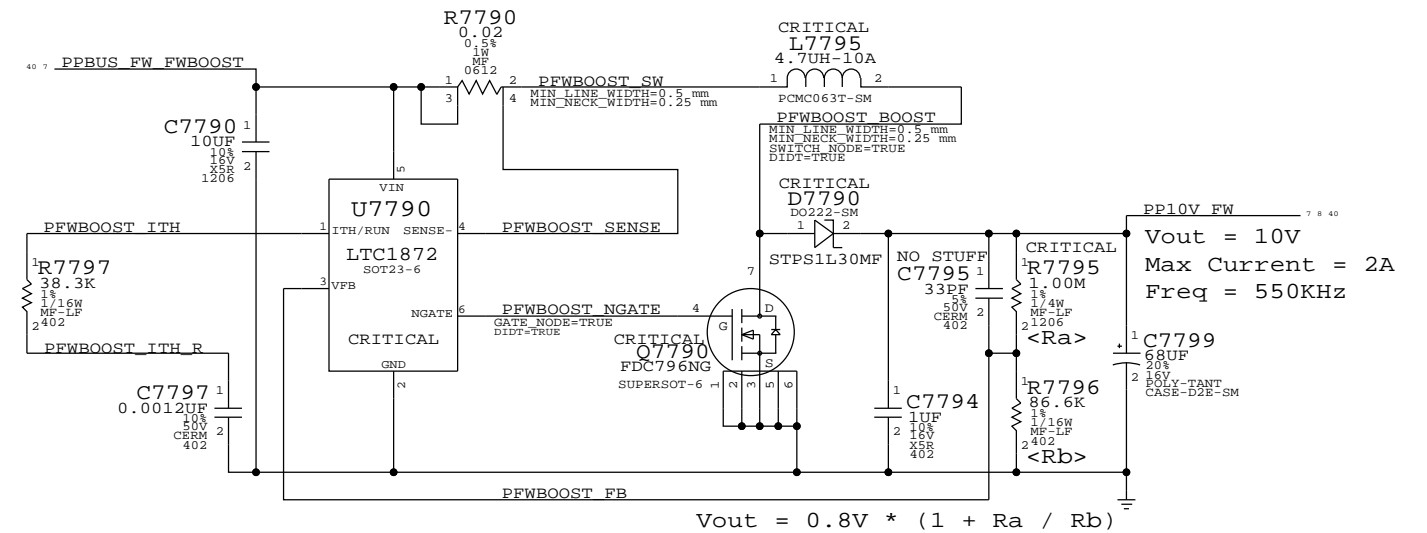




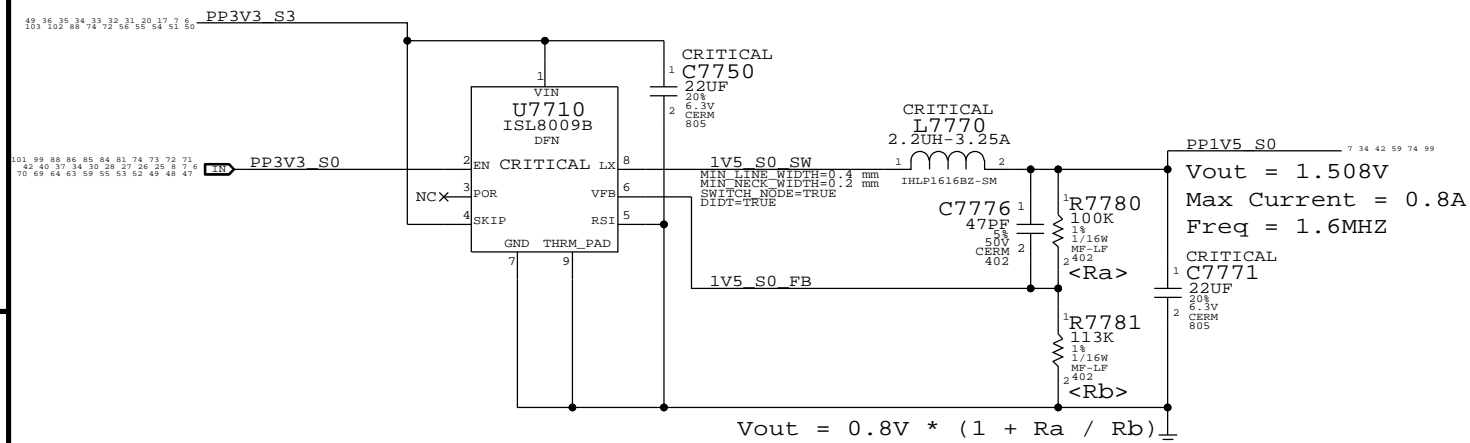
1.8V S0 Regulator



FW 10V Boost Regulator

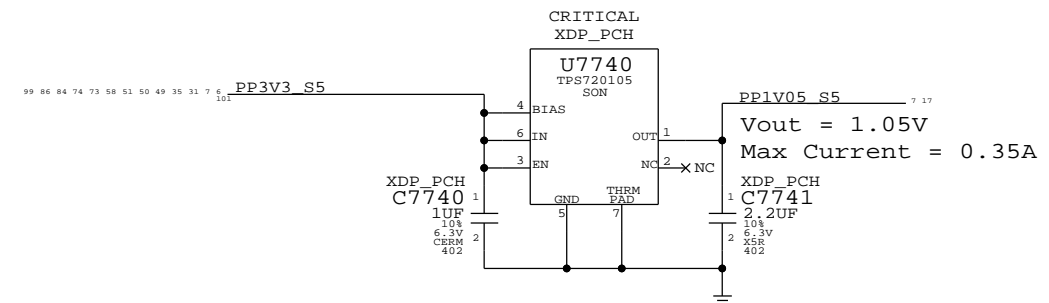


1.5V S0 Regulator

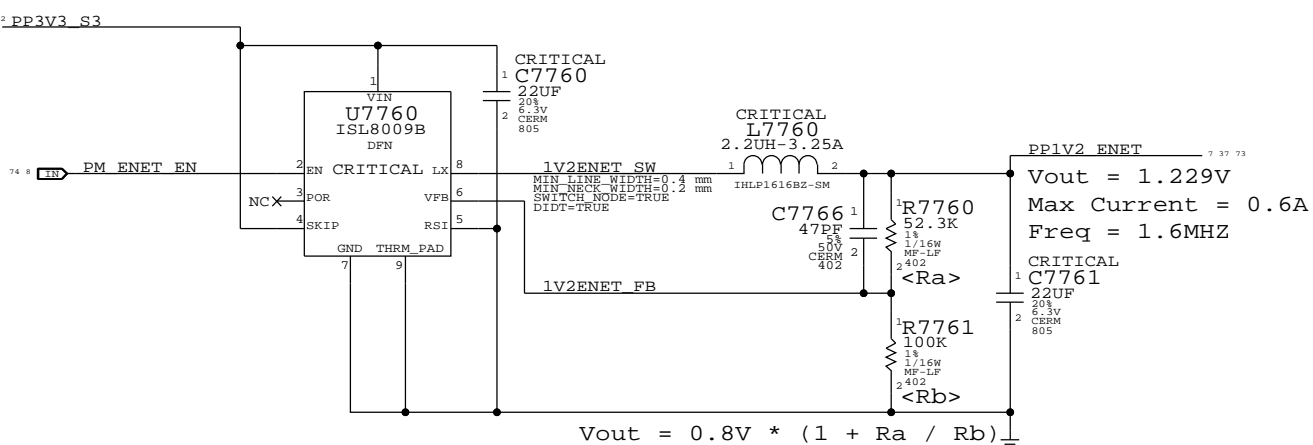


1.05V S5 LDO

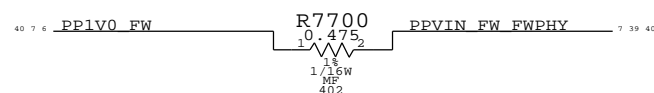
Ibex Peak-M requires JTAG pull-ups to be powered at 1.05V in S5. Pull-ups (3) must be 51 ohms to support XDP (not required in production). 70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.




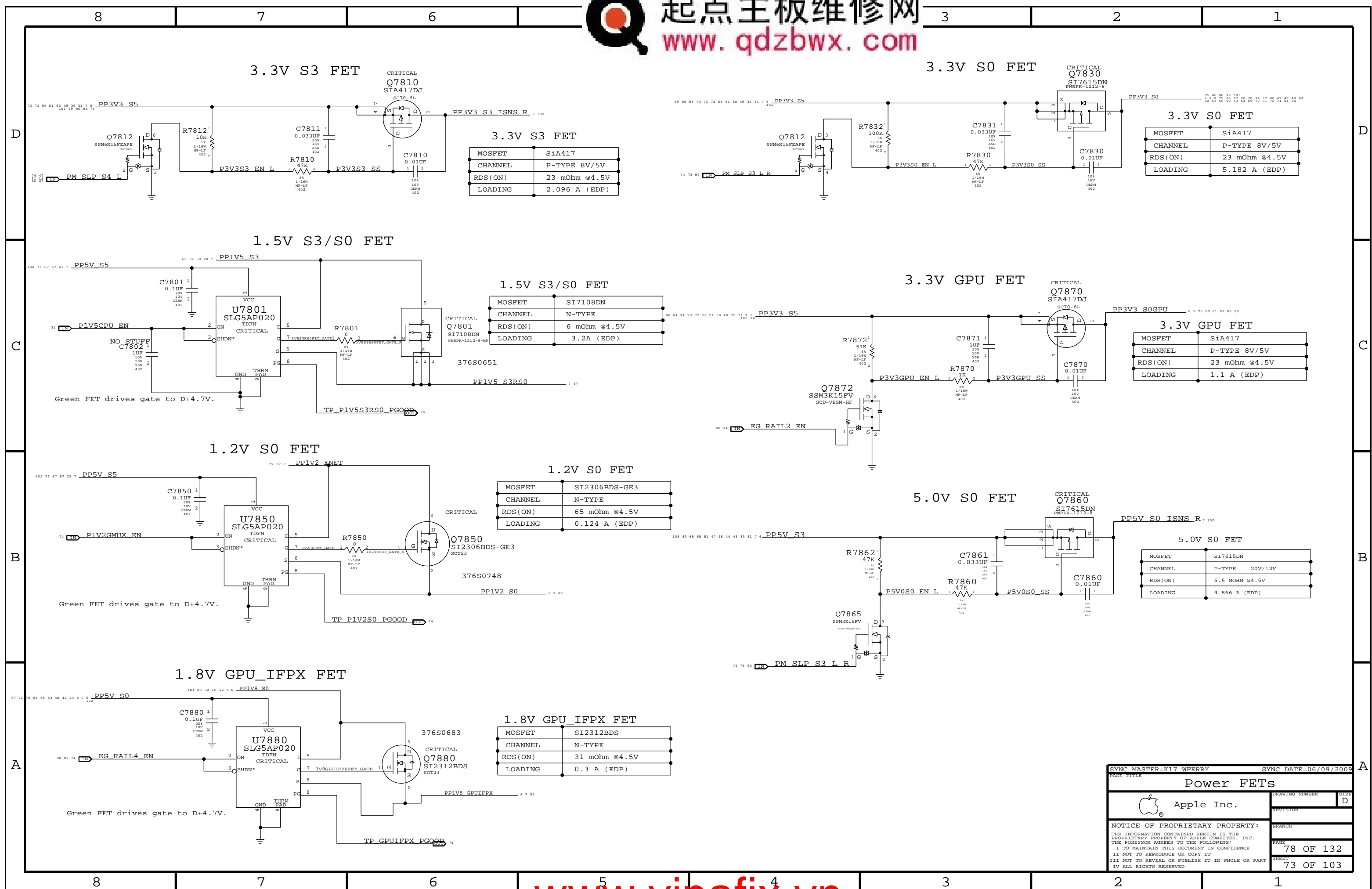
1.2V ENET Regulator



1.05V to 1.0V FW Drop

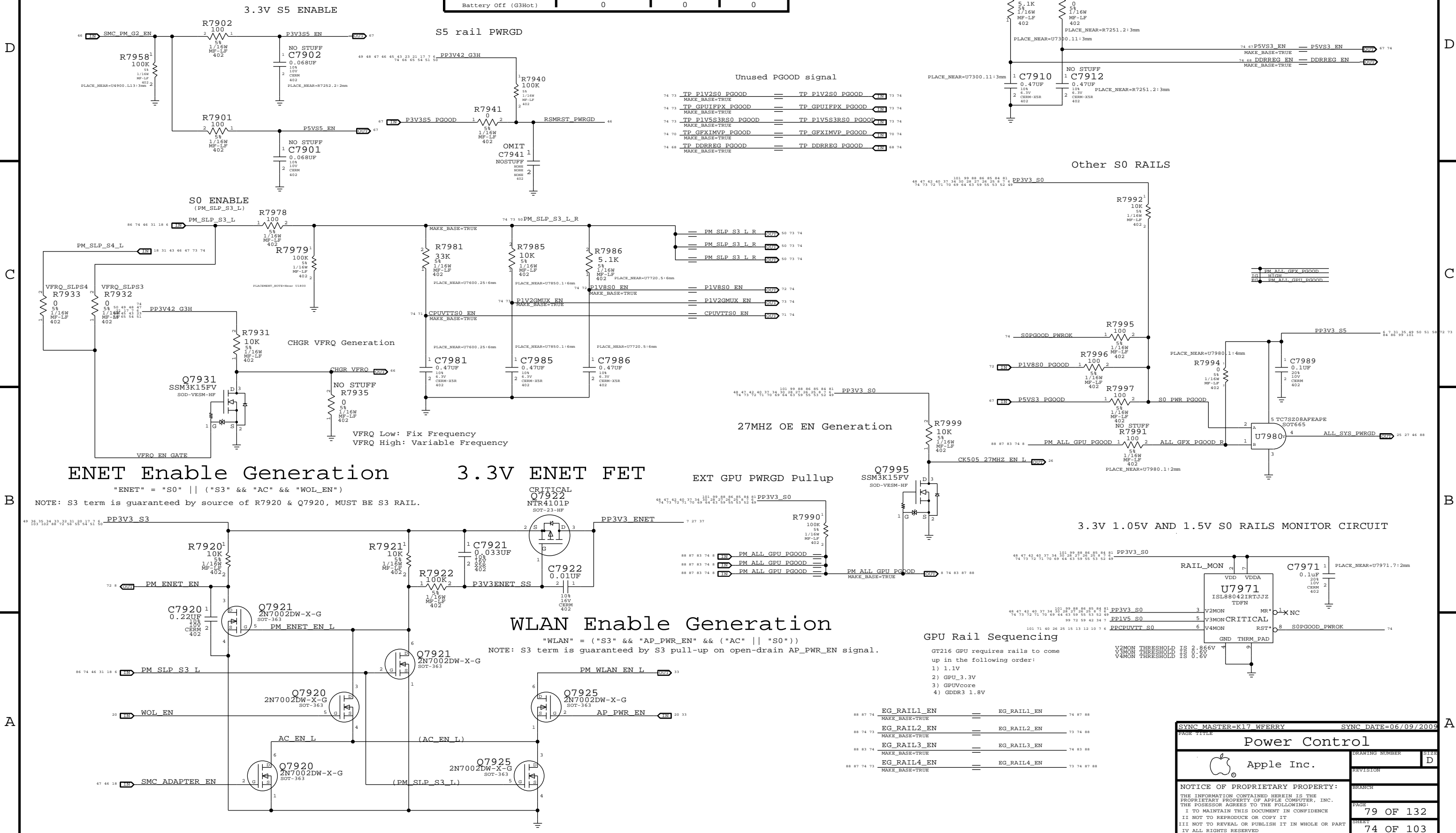


SYNC MASTER=K17 WFERRY		SYNC DATE=06/09/2009	
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Misc Power Supplies			
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State	SMC_PM_G2_E		
Run (S0)	1		
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0



SYNC MASTER=K17 WFERRY

SYNC DATE=06/09/2009

Power Control

Apple Inc.

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Page Notes

Power aliases required by this page:

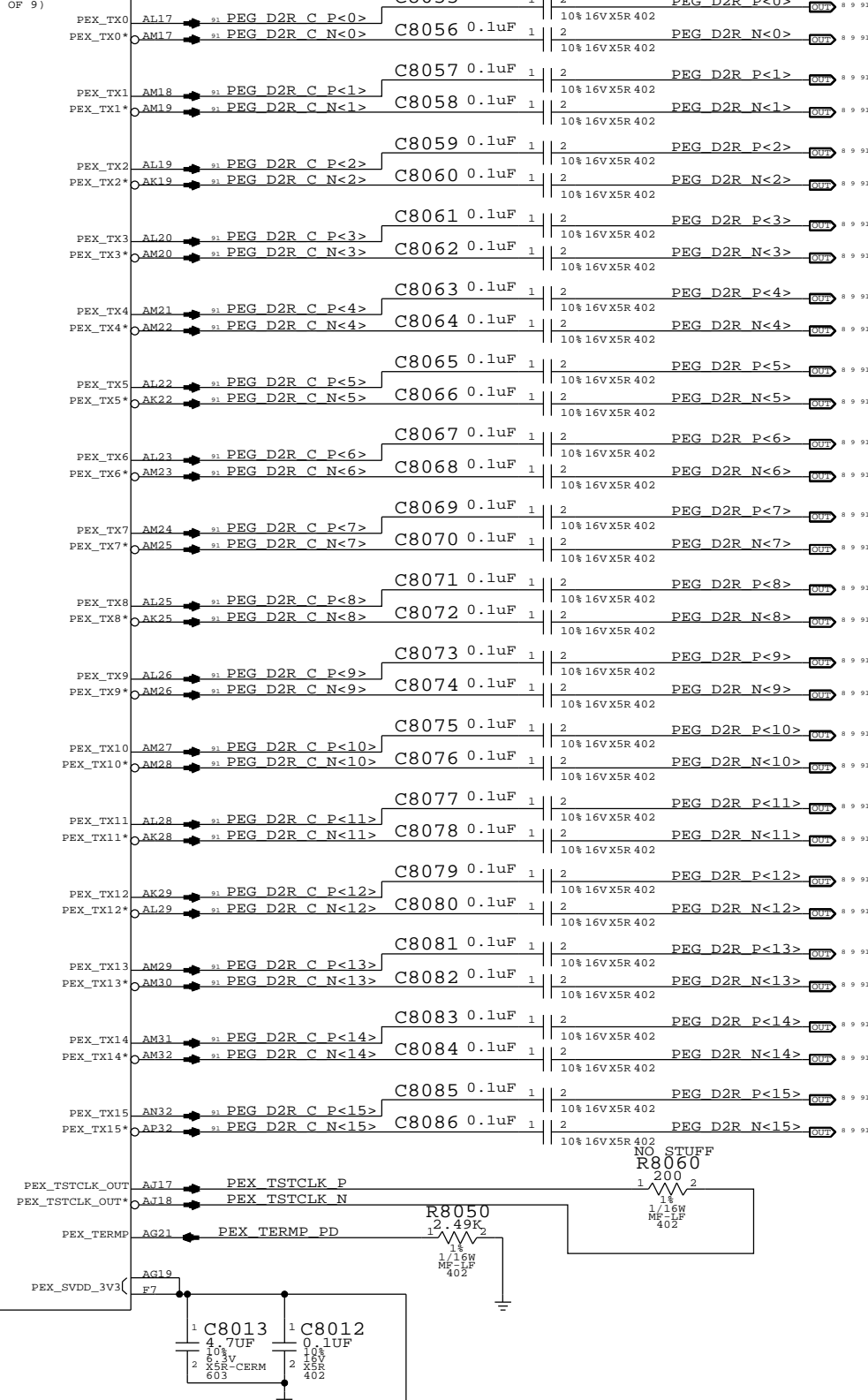
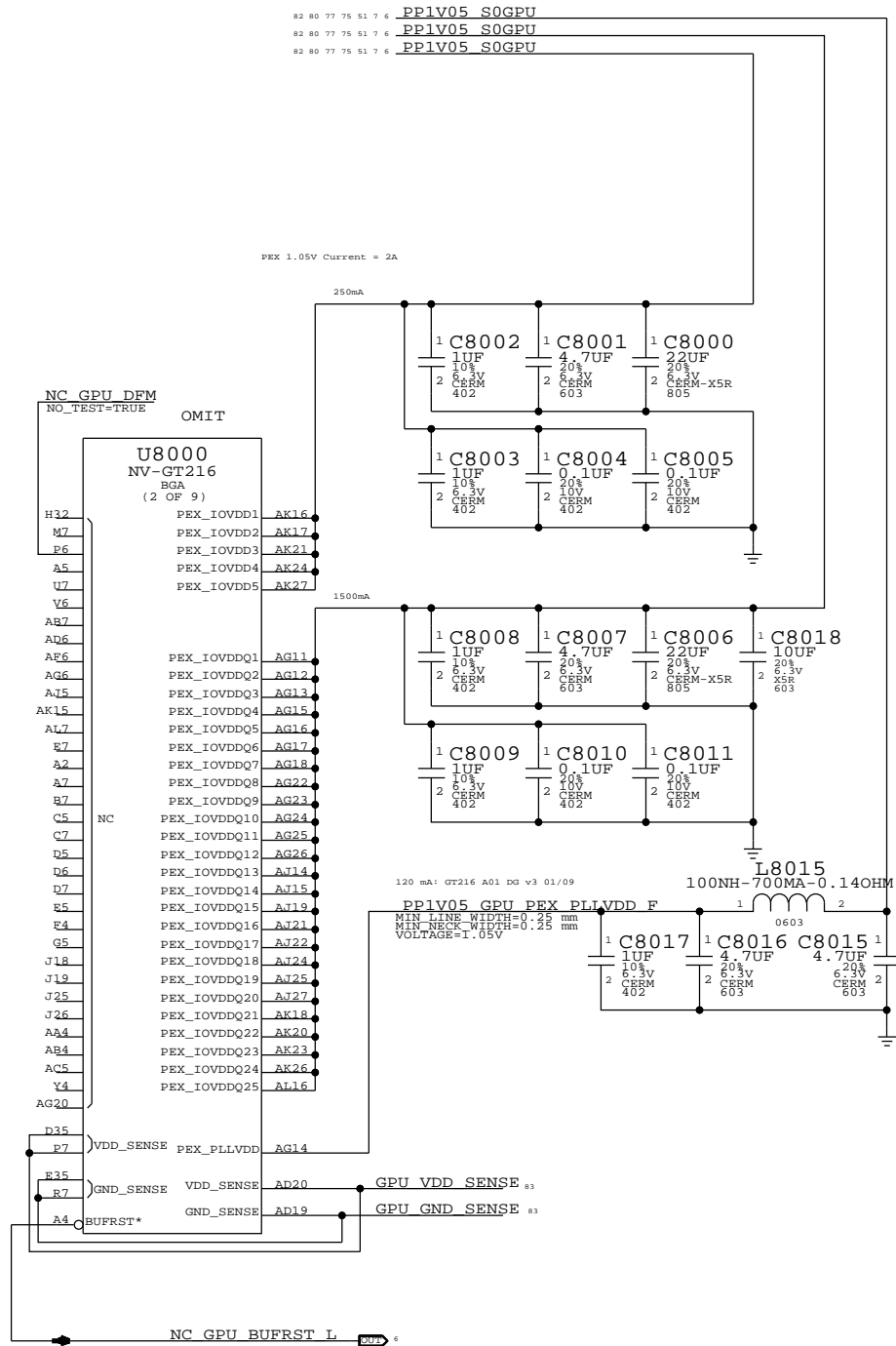
- =PP1V2_GPU_PEX_PL1XVDD
- =PP1V2_GPU_PEX_I0VDDQ
- =PP1V2_GPU_PEX_I0VDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)



SYNC MASTER=K18 MLB		SYNC DATE=06/29/2009	
PAGE TITLE		NV GT216 PCI-E	
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Page Notes

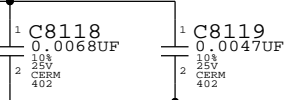
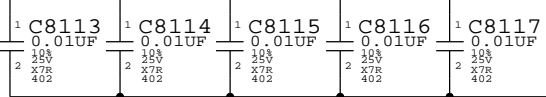
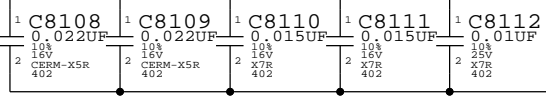
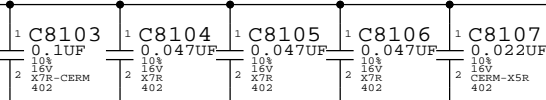
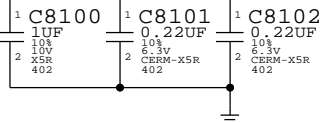
Power aliases required by this page:
- =PPVCORE_GPU
- =PPIV8_GPU_FBVDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

PPVCORE_GPU

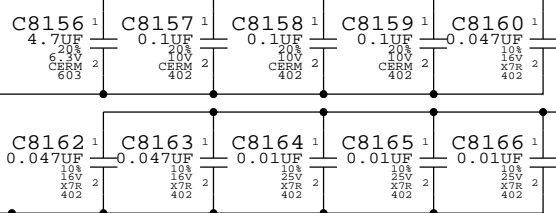
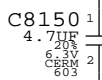
???A @ ???/???MHz Core/Mem Clk for VDD



PPIV8_S0GPU_ISNS

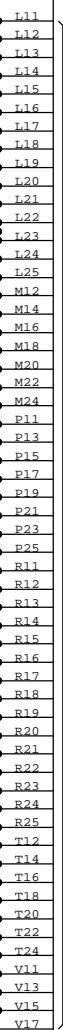
Nvidia PRD for GB-128 uses 4x4.7uF, 8x0.47uF, 16x0.1uF

???A @ ???/???MHz 1.8V GDDR3



NV-GT216
BGA
(9 OF 9)

OMIT

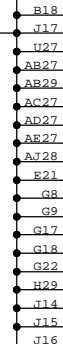


VDD

VDD

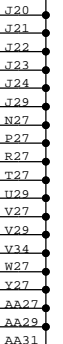
OMIT

U8000
NV-GT216
(7 OF 9)



FBVDDQ

FBVDDQ



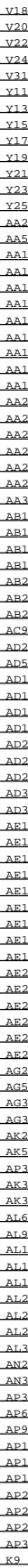
BGA
(8 OF 9)

OMIT



GND

GND



8

7

6


5

4

3

2

1

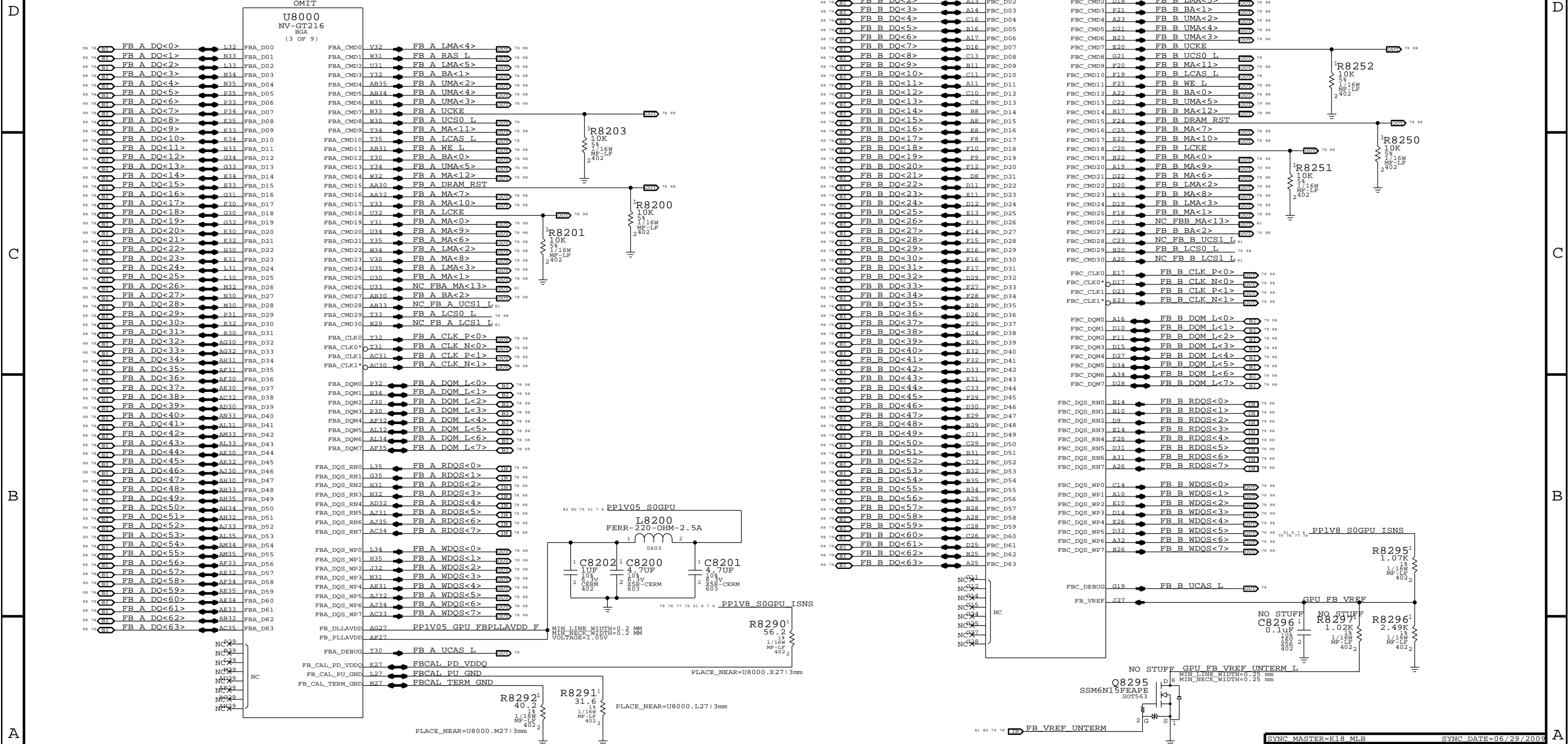
SYNC MASTER=GT216		SYNC DATE=03/26/2009	
PAGE TITLE			
NV GT216 CORE/FB POWER		DRAWING NUMBER	SIZE
 Apple Inc.		REVISION	D
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```
Power aliases required by this page:
- =PPIV2_GPU_FBPFLAVDD
- =PPIV8_GPU_FBIO

Signal aliases required by this page:
(NONE)

ROM options provided by this page:
(NONE)
```



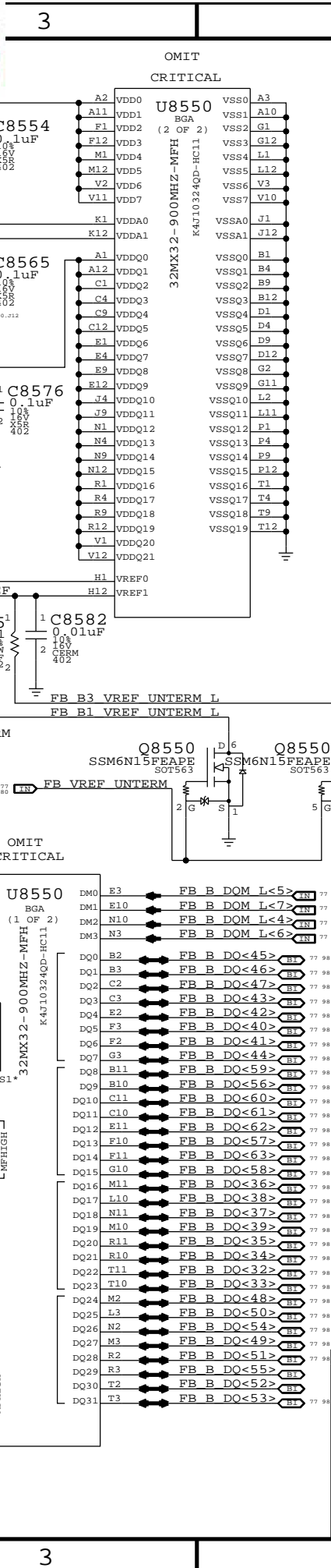
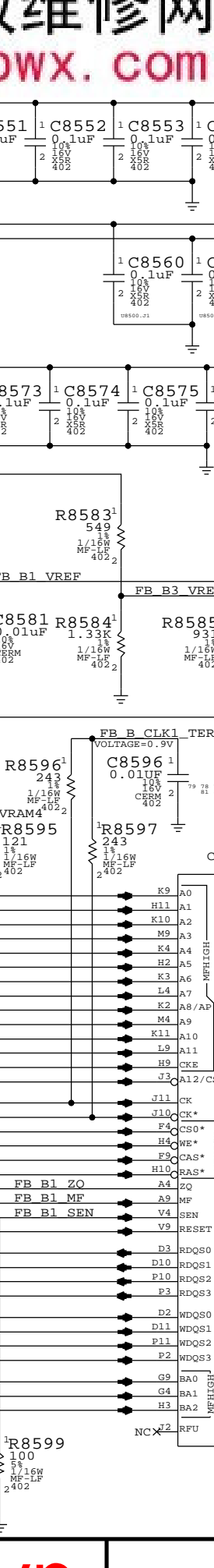
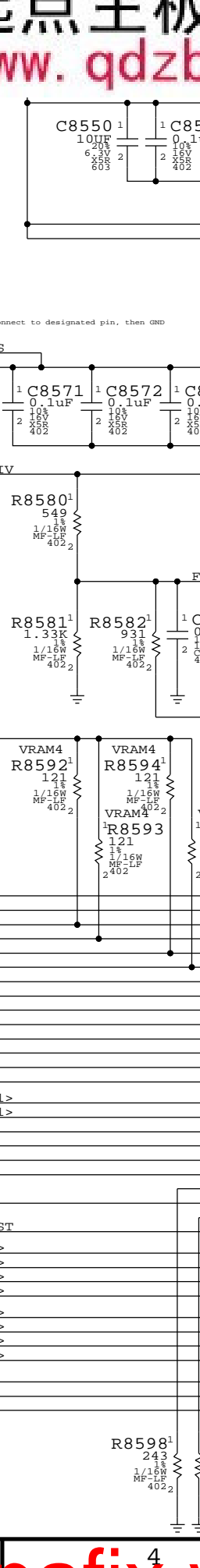
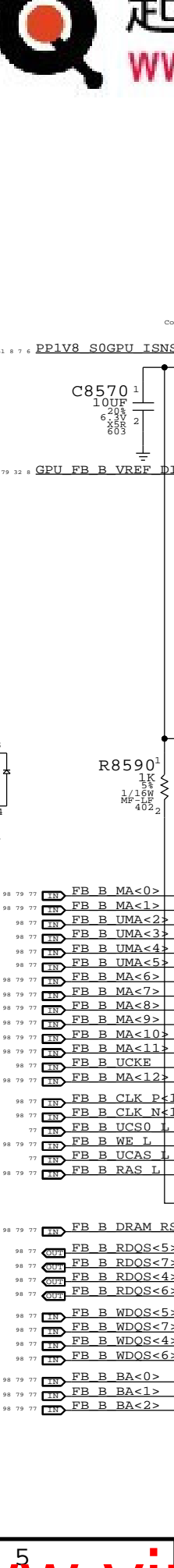
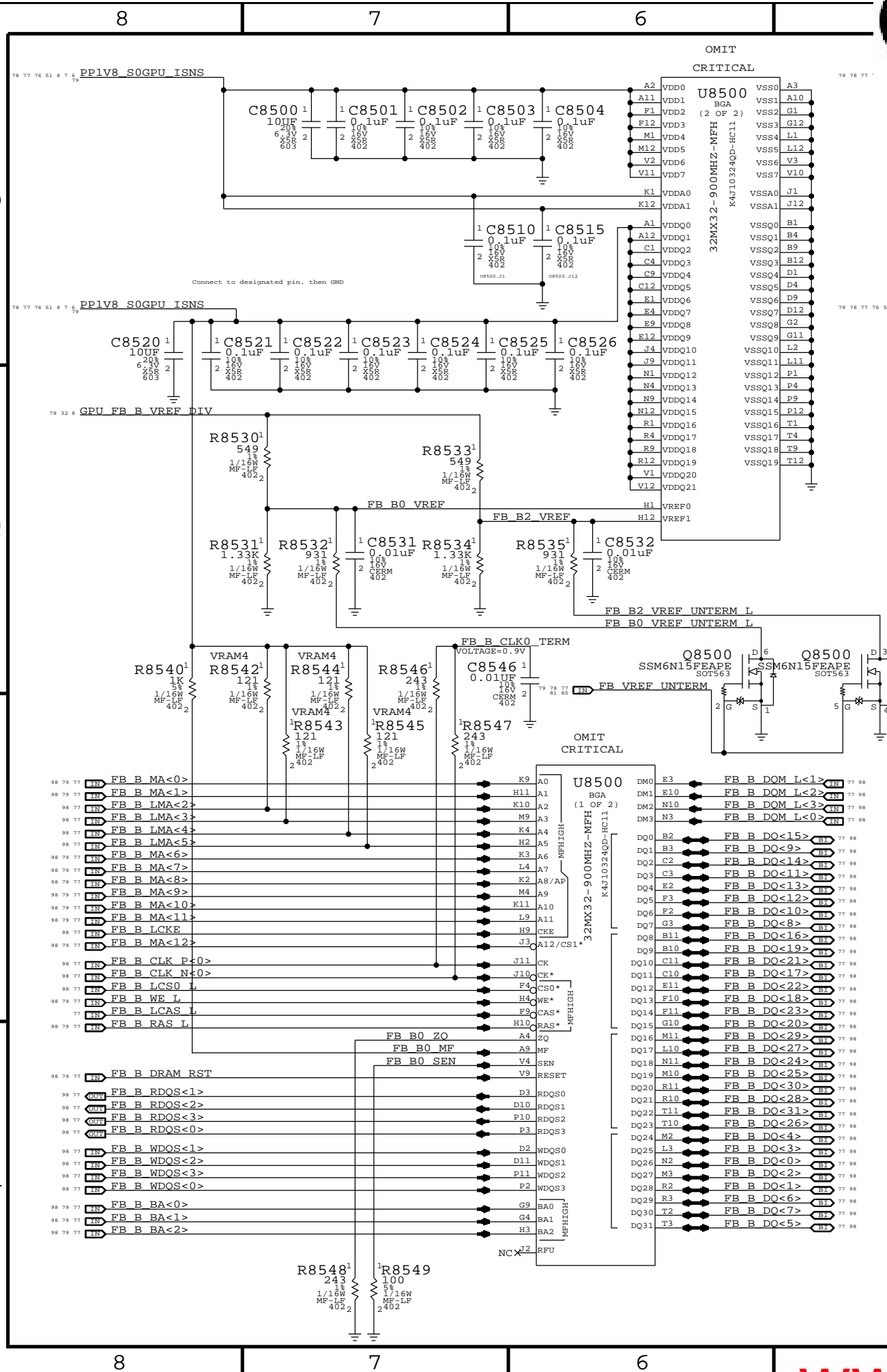
SYNC MASTER-K18 MLB		SYNC DATE=06/29/2009	
PAGE TITLE			
NV GT216 FRAME BUFFER I/F			
 Apple Inc.		DRAWING NUMBER	
		SIZE	
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Power aliases required by this page:
- PPIV8_S0GPU_VDD
- PPIV8_S0GPU_VREF_B

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
VRAM4



Page Notes

Power aliases required by this page:
- PPIV8_S0GPU_VDD
- PPIV8_S0GPU_VREF_B

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
VRAM4

SYNC MASTER=GT216

SYNC DATE=03/26/2009

GDDR3 Frame Buffer B (Top)

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Page Notes

Power aliases required by this page:

- =PP3V3_GPU_VDD33
- =PP3V3_GPU_MIO
- =PP1V2_GPU_PLLVDD
- =PP1V2_GPU_M_PLLVDD
- =PP1V2_GPU_VID_PLLVDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)


110mA

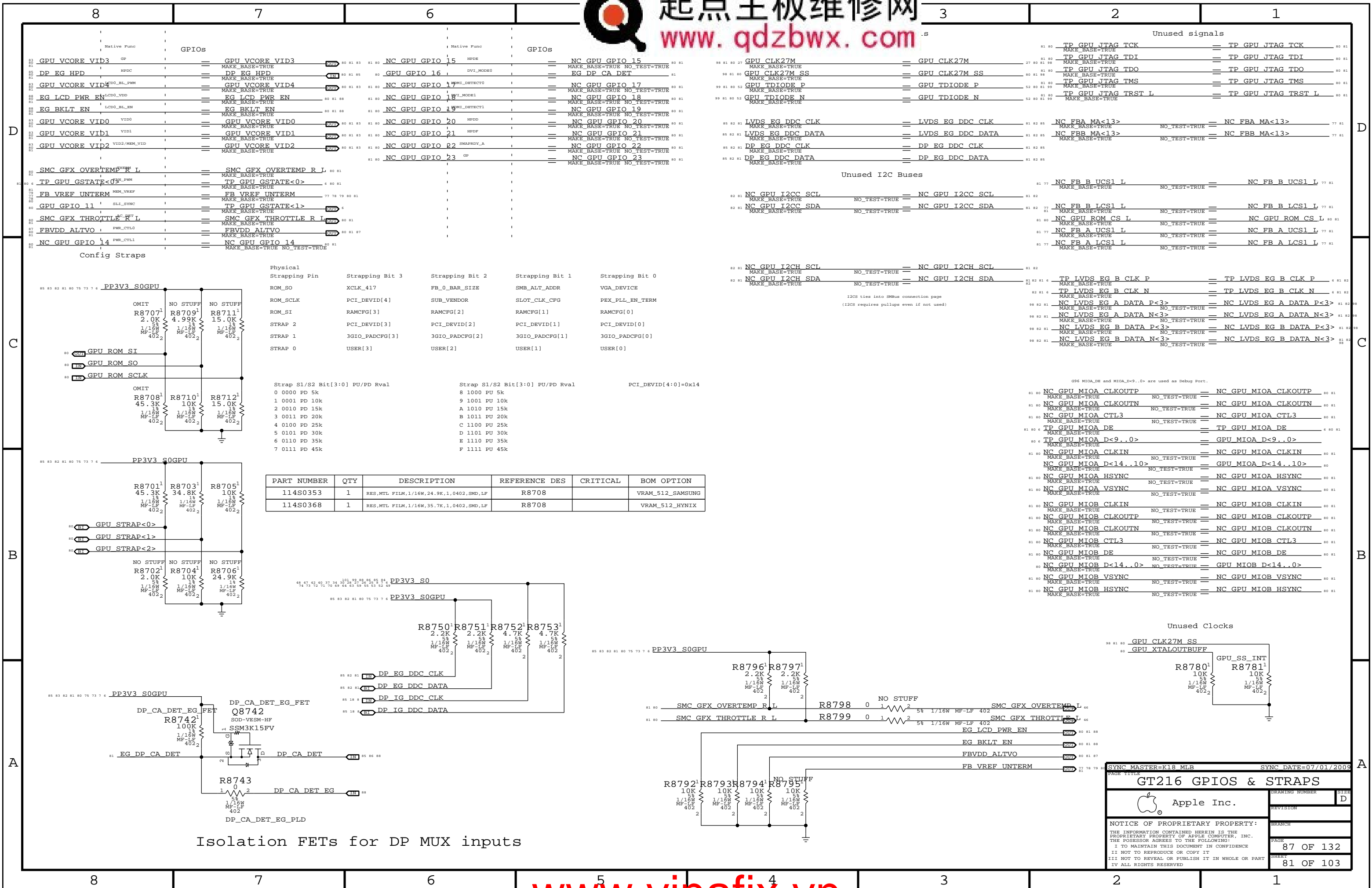
NV-GT216
BGA
(6 OF 9)

GPIO0	K1	GPU VCORE VID3	81	83
GPIO1	K2	DP EG HPD	81	85
GPIO2	K3	GPU VCORE VID4	81	83
GPIO3	H3	EG LCD PWR EN	81	88
GPIO4	H2	EG BKLT EN	81	88
GPIO5	H1	GPU VCORE VID0	81	83
GPIO6	H4	GPU VCORE VID1	81	83
GPIO7	H5	GPU VCORE VID2	81	83
GPIO8	H6	SMC GFX OVERTEMP R	81	83
GPIO9	J7	TP GPU GSTATE<0>	81	81
GPIO10	K4	FB VREF UNTERM	81	77 78 79 81
GPIO11	K5	GPU GPIO 11	81	81
GPIO12	H7	SMC GFX THROTTLE P	81	81
GPIO13	J4	FBVDD ALTVO	81	87
GPIO14	J6	NC GPU GPIO 14	81	81
GPIO15	L1	NC GPU GPIO 15	81	81
GPIO16	L2	GPU GPIO 16	81	81
GPIO17	L4	NC GPU GPIO 17	81	81
GPIO18	M4	NC GPU GPIO 18	81	81
GPIO19	L7	NC GPU GPIO 19	81	81
GPIO20	L5	NC GPU GPIO 20	81	81
GPIO21	K6	NC GPU GPIO 21	81	81
GPIO22	L6	NC GPU GPIO 22	81	81
GPIO23	M6	NC GPU GPIO 23	81	81

JTAG_TCK	AP14	TP GPU JTAG TCK	81	81
JTAG_TDI	AN14	TP GPU JTAG TDI	81	81
JTAG_TDO	AN16	TP GPU JTAG TDO	81	81
JTAG_TMS	AR14	TP GPU JTAG TMS	81	81
JTAG_TRST*	AP16	TP GPU JTAG TRST	81	81
MIOA_CLKIN	N4	NC GPU MIOA CLKIN	81	81
MIOA_CLKOUT	R4	NC GPU MIOA CLKOUT	81	81
MIOA_CLKOUT*	T4	NC GPU MIOA CLKOUT	81	81
MIOA_CTL3	P5	NC GPU MIOA CTL3	81	81
MIOA_DE	N2	TP GPU MIOA DE	81	81
MIOA_D0	N1	TP GPU MIOA D<0>	81	81
MIOA_D1	P4	TP GPU MIOA D<1>	81	81
MIOA_D2	P1	TP GPU MIOA D<2>	81	81
MIOA_D3	P2	TP GPU MIOA D<3>	81	81
MIOA_D4	P3	TP GPU MIOA D<4>	81	81
MIOA_D5	T3	TP GPU MIOA D<5>	81	81
MIOA_D6	T2	TP GPU MIOA D<6>	81	81
MIOA_D7	T1	TP GPU MIOA D<7>	81	81
MIOA_D8	U4	TP GPU MIOA D<8>	81	81
MIOA_D9	U1	TP GPU MIOA D<9>	81	81
MIOA_D10	U2	GPU MIOA D<10>	81	81
MIOA_D11	U3	GPU MIOA D<11>	81	81
MIOA_D12	R6	GPU MIOA D<12>	81	81
MIOA_D13	T6	GPU MIOA D<13>	81	81
MIOA_D14	N6	GPU MIOA D<14>	81	81
MIOA_HSYNC	N3	NC GPU MIOA HSYNC	81	81
MIOA_VSYNC	L3	NC GPU MIOA VSYNC	81	81
MIOB_CLKIN	AE1	NC GPU MIOB CLKIN	81	81
MIOB_CLKOUT	V4	NC GPU MIOB CLKOUT	81	81
MIOB_CLKOUT*	M4	NC GPU MIOB CLKOUT	81	81
MIOB_CTL3	M3	NC GPU MIOB CTL3	81	81
MIOB_DE	Y5	NC GPU MIOB DE	81	81
MIOB_D0	Y1	NC GPU MIOB D<0>	81	81
MIOB_D1	Y2	NC GPU MIOB D<1>	81	81
MIOB_D2	Y3	NC GPU MIOB D<2>	81	81
MIOB_D3	AB3	NC GPU MIOB D<3>	81	81
MIOB_D4	AB2	NC GPU MIOB D<4>	81	81
MIOB_D5	AB1	NC GPU MIOB D<5>	81	81
MIOB_D6	AC4	NC GPU MIOB D<6>	81	81
MIOB_D7	AC1	NC GPU MIOB D<7>	81	81
MIOB_D8	AC2	NC GPU MIOB D<8>	81	81
MIOB_D9	AC3	NC GPU MIOB D<9>	81	81
MIOB_D10	AE3	NC GPU MIOB D<10>	81	81
MIOB_D11	AE2	NC GPU MIOB D<11>	81	81
MIOB_D12	U6	NC GPU MIOB D<12>	81	81
MIOB_D13	M6	NC GPU MIOB D<13>	81	81
MIOB_D14	Y6	NC GPU MIOB D<14>	81	81

MIOB_HSYNC	W1	NC GPU MIOB HSYNC	81	81
MIOB_VSYNC	W2	NC GPU MIOB VSYNC	81	81
THERMDP	B5	GPU TDIODE P	81	99
THERMDN	B4	GPU TDIODE N	81	99

SYNC MASTER=K18 MLB		SYNC DATE=06/29/2009	
PAGE TITLE			
NV GT216 GPIO/MIO/MISC			
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Isolation FETs for DP MUX inputs

SYNC MASTER=K18 MLB

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GT216 GPIOs & STRAPS	
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8

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1

Page Notes

Power aliases required by this page:
- =PP1V8_GPU_IPFX
- =PP3V3_GPU_IPPCD_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Sum of peak currents: 240mA

73 7 6 PP1V8 GPUIPFX

L8800
FERR-220-OHM-2.5A

7mA peak per diff pair
7mA peak for all pairs

C8800 4.7UF 20% 6.3V CERM 603
C8801 0.1UF 20% 10V CERM 402
C8803 0.1UF 20% 10V CERM 402

PP1V8 GPU IPFAB IOVDD F
MIN LINE WIDTH=0.4 mm
MIN NECK WIDTH=0.2 mm
VOLTAGE=1.8V

OMIT

U8000
NV-GT216
BGA
(5 OF 9)

IFPA_TXC* AM11 LVDS EG A CLK P 88 98
IFPA_TXC* AM12 LVDS EG A CLK N 88 98
IFPA_TXD0* AM8 LVDS EG A DATA P<0> 88 98
IFPA_TXD1* AM10 LVDS EG A DATA N<0> 88 98
IFPA_TXD1* AM10 LVDS EG A DATA P<1> 88 98
IFPA_TXD1* AM9 LVDS EG A DATA N<1> 88 98
IFPA_TXD2* AK10 LVDS EG A DATA P<2> 88 98
IFPA_TXD2* AL10 LVDS EG A DATA N<2> 88 98
IFPA_TXD3* AK11 NC LVDS EG A DATA P<3> 81 98
IFPA_TXD3* AL11 NC LVDS EG A DATA N<3> 81 98
IFPB_TXC* AP13 TP LVDS EG B CLK P 6 81
IFPB_TXC* AN13 TP LVDS EG B CLK N 6 81
IFPB_TXD4* AN8 LVDS EG B DATA P<0> 88 98
IFPB_TXD4* AP8 LVDS EG B DATA N<0> 88 98
IFPB_TXD5* AP10 LVDS EG B DATA P<1> 88 98
IFPB_TXD5* AN10 LVDS EG B DATA N<1> 88 98
IFPB_TXD6* AR11 LVDS EG B DATA P<2> 88 98
IFPB_TXD6* AR10 LVDS EG B DATA N<2> 88 98
IFPB_TXD7* AN11 NC LVDS EG B DATA P<3> 81 98
IFPB_TXD7* AP11 NC LVDS EG B DATA N<3> 81 98
IFPC_AUX_I2CW_SCL AP2 DP EG AUX CH P 85 98
IFPC_AUX_I2CW_SDA* AN3 DP EG AUX CH N 85 98
IFPC_L0* AM7 DP EG ML P<0> 85 98
IFPC_L0* AM6 DP EG ML N<0> 85 98
IFPC_L1* AL5 DP EG ML P<1> 85 98
IFPC_L1* AM5 DP EG ML N<1> 85 98
IFPC_L2* AM3 DP EG ML P<2> 85 98
IFPC_L2* AM4 DP EG ML N<2> 85 98
IFPC_L3* AP1 DP EG ML P<3> 85 98
IFPC_L3* AR2 DP EG ML N<3> 85 98
IFPD_AUX_I2CX_SCL AK1 NC
IFPD_AUX_I2CX_SDA* AN1 NC
IFPD_L0* AK1 NC
IFPD_L0* AK1 NC
IFPD_L1* AK1 NC
IFPD_L1* AK1 NC
IFPD_L2* AK1 NC
IFPD_L2* AK1 NC
IFPD_L3* AK1 NC
IFPD_L3* AK1 NC
IFPE_AUX_I2CY_SCL AK1 NC
IFPE_AUX_I2CY_SDA* AN1 NC
IFPE_L0* AK1 NC
IFPE_L0* AK1 NC
IFPE_L1* AK1 NC
IFPE_L1* AK1 NC
IFPE_L2* AK1 NC
IFPE_L2* AK1 NC
IFPE_L3* AK1 NC
IFPE_L3* AK1 NC
IFPF_AUX_I2CZ_SCL AK1 NC
IFPF_AUX_I2CZ_SDA* AN1 NC
IFPF_L0* AK1 NC
IFPF_L0* AK1 NC
IFPF_L1* AK1 NC
IFPF_L1* AK1 NC
IFPF_L2* AK1 NC
IFPF_L2* AK1 NC
IFPF_L3* AK1 NC
IFPF_L3* AK1 NC
DACA_RED AK1 NC
DACA_GREEN AK1 NC
DACA_BLUE AK1 NC
DACA_HSYNC AK1 NC
DACA_VSYNC AK1 NC
DACB_RED AK1 NC
DACB_GREEN AK1 NC
DACB_BLUE AK1 NC
CEC AK1 NC
DACB_HSYNC AK1 NC
DACB_VSYNC AK1 NC

NO STUFF
R8861 1K 5% 1/16W MF-LP 402
NO STUFF
R8860 1K 5% 1/16W MF-LP 402

GPU IPFEF RSET 82
GPU IFPC RSET 82
GPU IPFAB RSET 82
GPU IFPD RSET 82

L8805
180-OHM-1.5A

C8805 4.7UF 20% 6.3V CERM 603
C8806 0.1UF 20% 10V CERM 402

PP1V05 GPU IPFCD IOVDD F 82
PP1V05 GPU IPFEF IOVDD F 82
PP1V05 GPU IPFAB PLLVDD F 82
GPU IPFAB RSET 82
PP3V3 GPU IFPC PLLVDD F 82
GPU IFPC RSET 82
PP1V8 GPU IPFEF PLLVDD F 82
GPU IPFEF RSET 82

L8810
180-OHM-1.5A

C8810 4.7UF 20% 6.3V CERM 603
C8811 0.1UF 20% 10V CERM 402
C8813 0.1UF 20% 10V CERM 402

LVDS EG DDC CLK 85 81
LVDS EG DDC DATA 85 81

L8815
FERR-220-OHM-2.5A

C8815 4.7UF 20% 6.3V CERM 603
C8816 0.1UF 20% 10V CERM 402

NC GPU I2CC_SCL 81 81
NC GPU I2CC_SDA 81 81

SMBUS_SMC_0_S5_SCL 82 49 44
SMBUS_SMC_0_S5_SDA 82 49 44

NC GPU I2CH_SDA 81 81
NC GPU I2CH_SCL 81 81

DP EG DDC CLK 85 81
DP EG DDC DATA 85 81

PP1V05 GPU IPFEF IOVDD F 82
MIN LINE WIDTH=0.4 mm
MIN NECK WIDTH=0.1 mm
VOLTAGE=1.05V

PP1V8 GPU IPFEF PLLVDD F 82
MIN LINE WIDTH=0.4 mm
MIN NECK WIDTH=0.1 mm
VOLTAGE=1.8V

R8856 10K 5% 1/16W MF-LP 402
R8857 10K 5% 1/16W MF-LP 402

GPU DACA VDD
GPU DACB VDD
PP1V8 GPU IPFD PLLVDD
MIN LINE WIDTH=0.4 mm
MIN NECK WIDTH=0.1 mm
VOLTAGE=1.8V

R8852 10K 5% 1/16W MF-LP 402
R8853 10K 5% 1/16W MF-LP 402
R8854 10K 5% 1/16W MF-LP 402

AG12 DACA_VDD
AG12 DACA_VREF
AG12 DACA_RSET

AG12 DACA_VDD
AG12 DACA_VREF
AG12 DACA_RSET

AG12 DACA_VDD
AG12 DACA_VREF
AG12 DACA_RSET

AG12 DACA_VDD
AG12 DACA_VREF
AG12 DACA_RSET


AG12 DACA_VDD
AG12 DACA_VREF
AG12 DACA_RSET

AG12 DACA_VDD
AG12 DACA_VREF
AG12 DACA_RSET

AG12 DACA_VDD
AG12 DACA_VREF
AG12 DACA_RSET

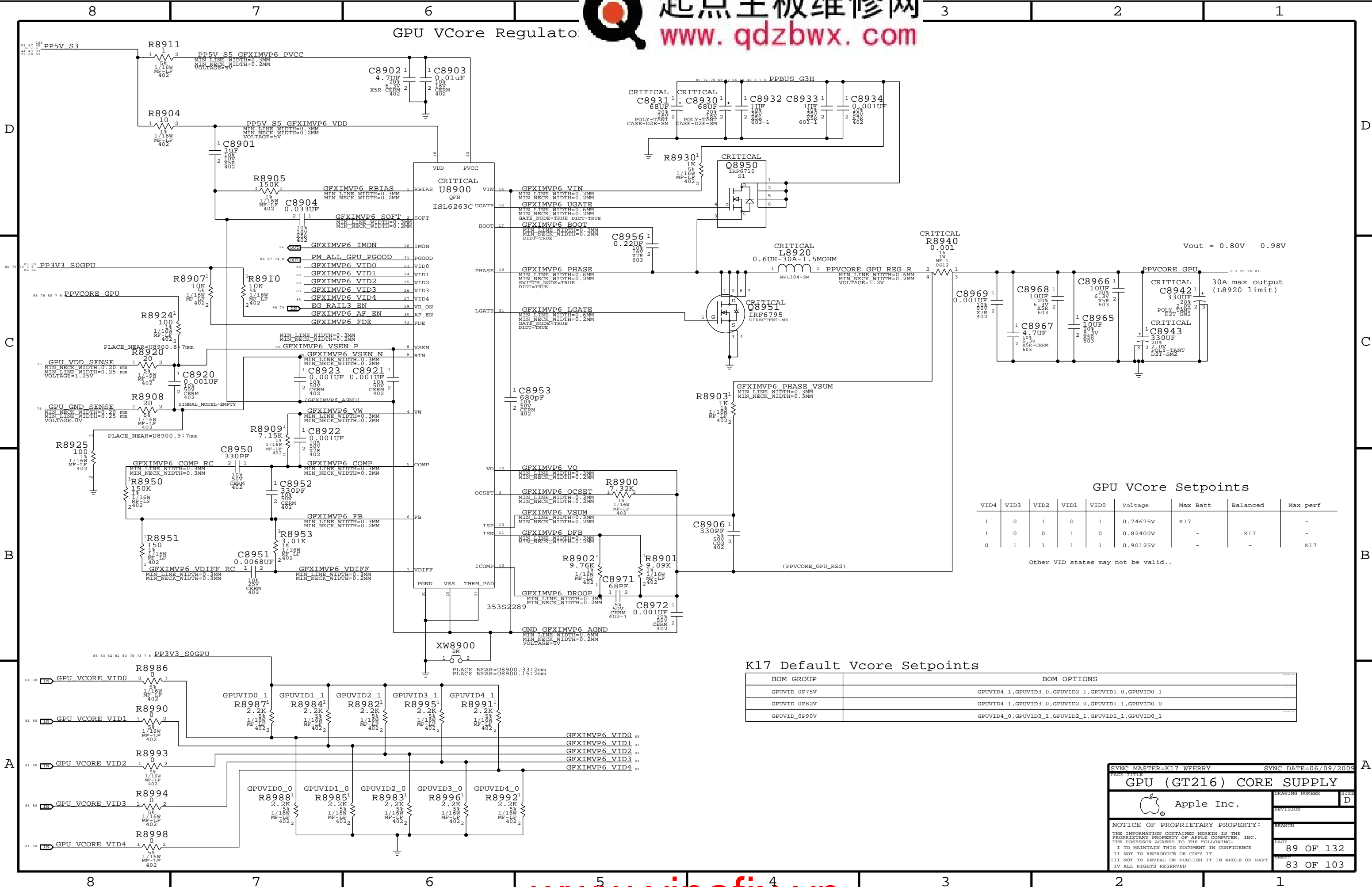
AG12 DACA_VDD
AG12 DACA_VREF
AG12 DACA_RSET

AG12 DACA_VDD
AG12 DACA_VREF
AG12 DACA_RSET

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NV GT216 VIDEO		INTERFACES	
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GPU VCore Regulator



GPU VCore Setpoints

VID4	VID3	VID2	VID1	VID0	Voltage	Max Batt	Balanced	Max perf
1	0	1	0	1	0.74675V	K17		-
1	0	0	1	0	0.82400V	-	K17	-
0	1	1	1	1	0.90125V	-	-	K17

Other VID states may not be valid..

K17 Default Vcore Setpoints

BOM GROUP	BOM OPTIONS
GPUVID_0P75V	GPUVID4_1, GPUVID3_0, GPUVID2_1, GPUVID1_0, GPUVID0_1
GPUVID_0P82V	GPUVID4_1, GPUVID3_0, GPUVID2_0, GPUVID1_1, GPUVID0_0
GPUVID_0P90V	GPUVID4_0, GPUVID3_1, GPUVID2_1, GPUVID1_1, GPUVID0_1

SYNC MASTER=K17.WFERRY

SYNC DATE=06/09/2009

GPU (GT216) CORE SUPPLY

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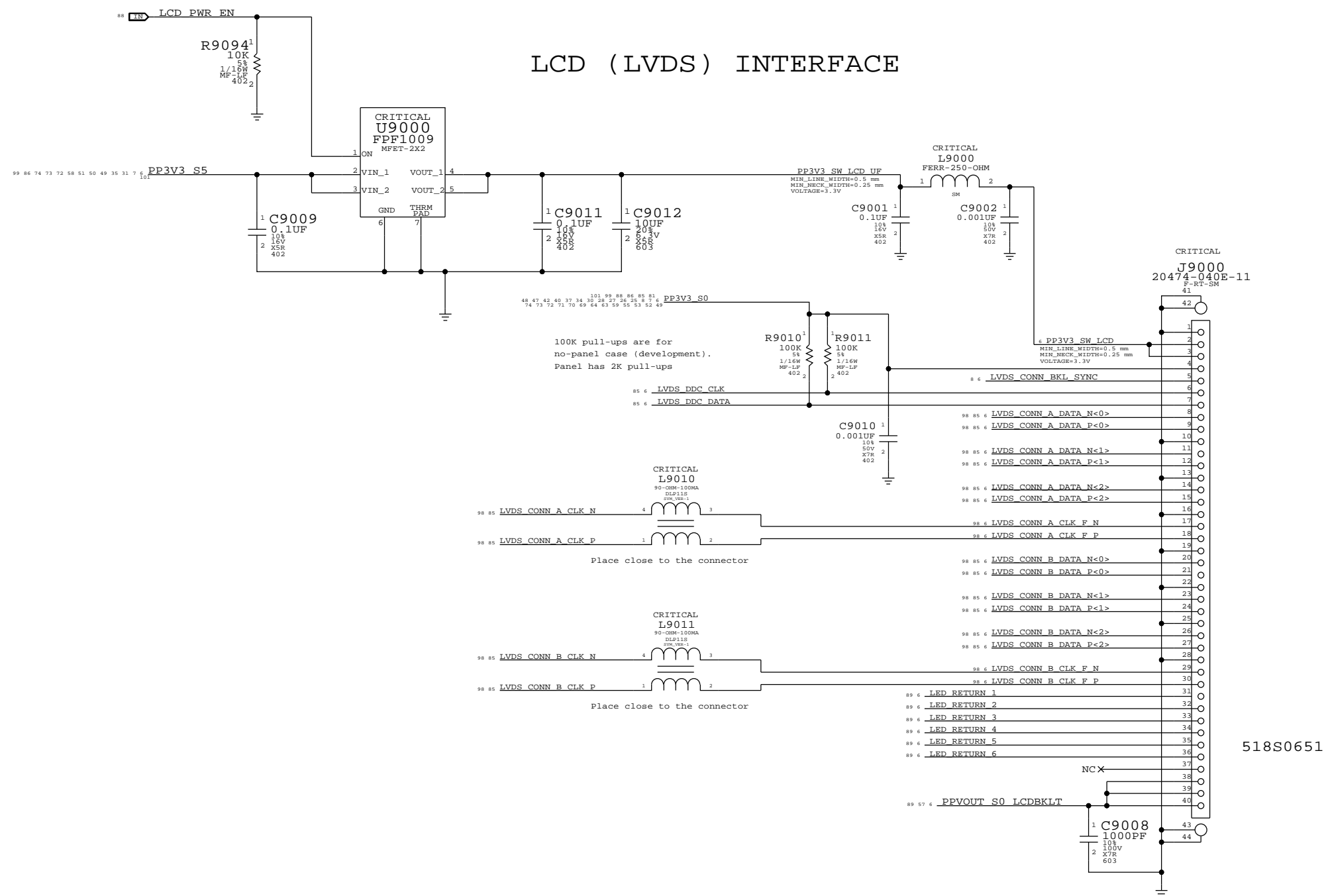
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LCD (LVDS) INTERFACE

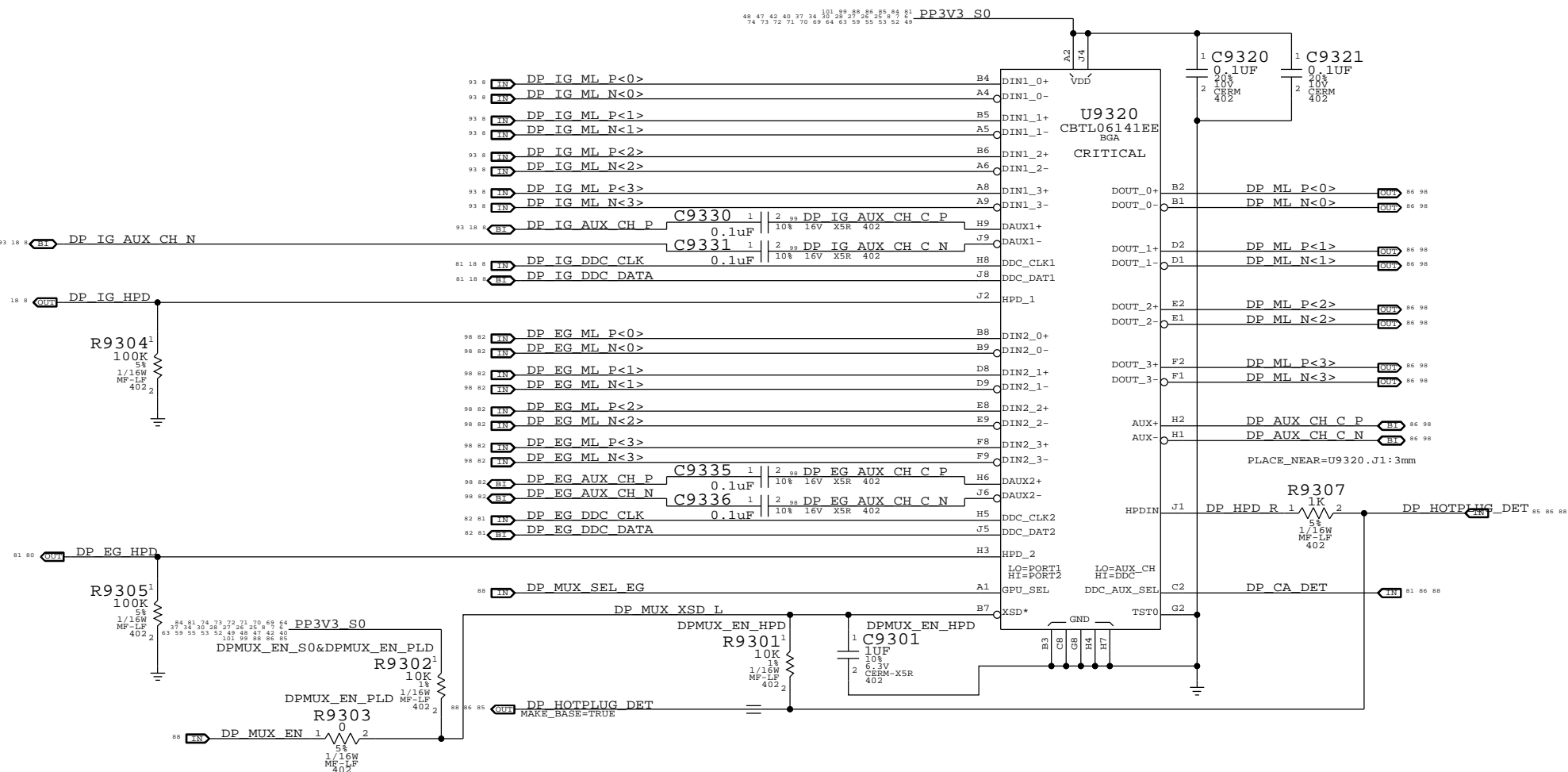
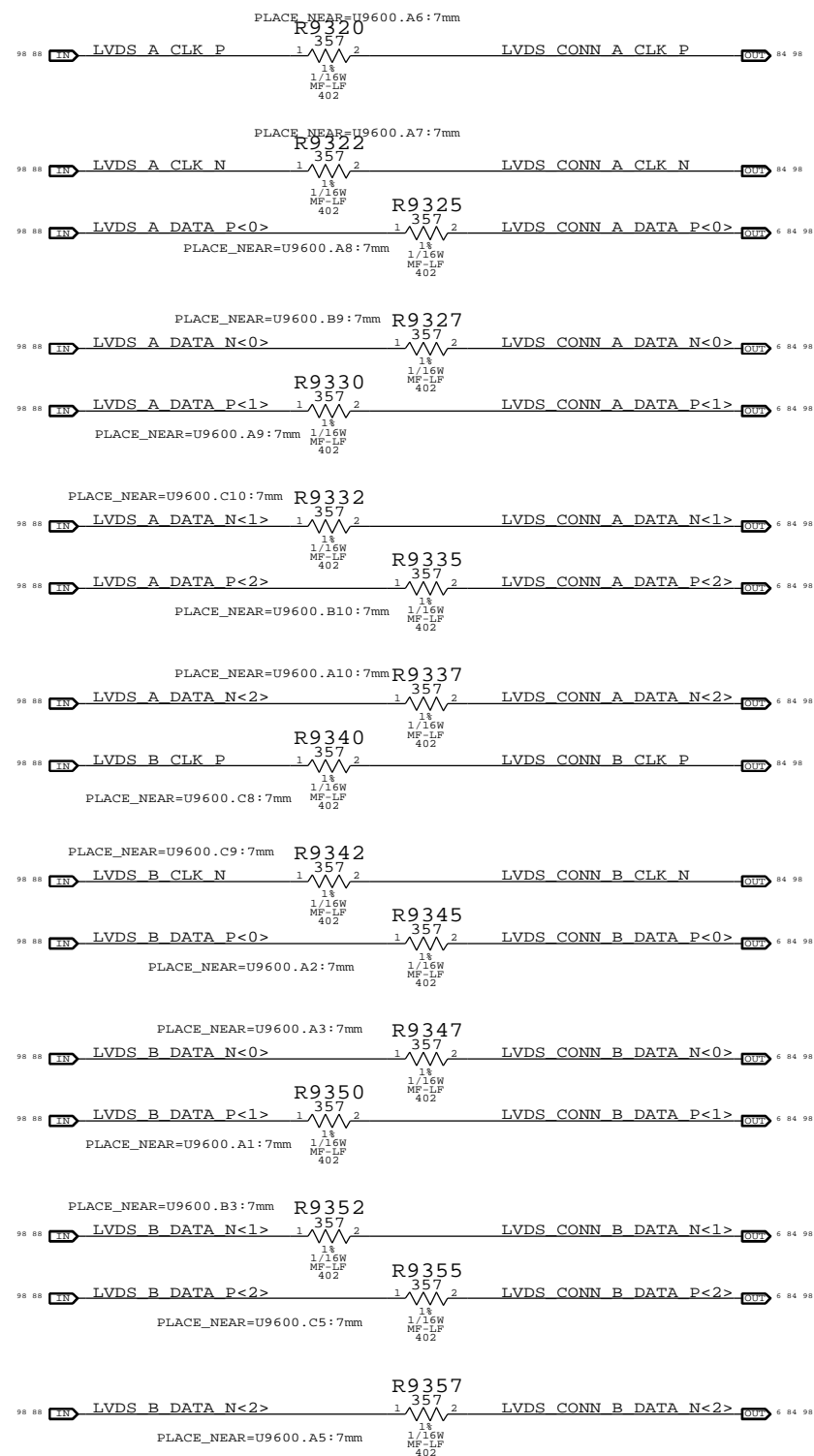


SYNC MASTER=K20A MLB		SYNC DATE=03/26/2009	
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LVDS Display Connector			
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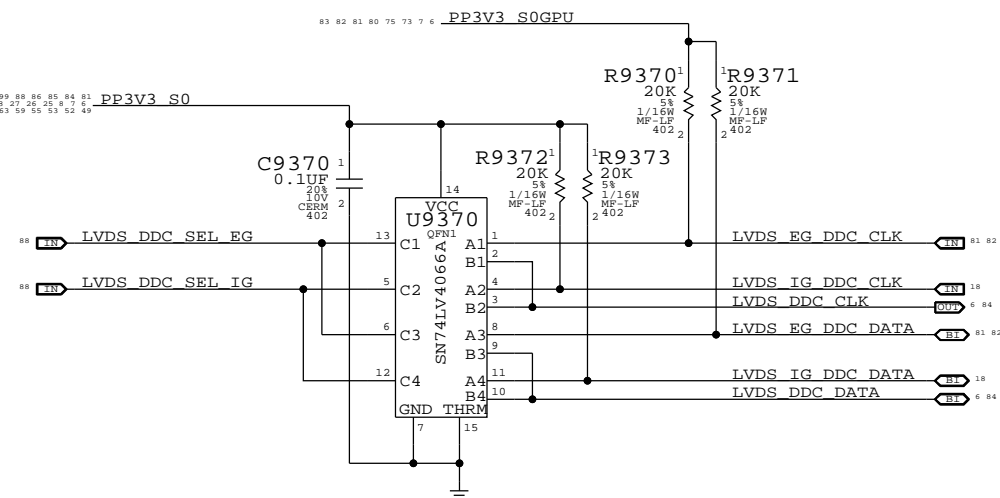
DisplayPort Mux


LVDS Transmitter Termination

All emulated LVDS outputs require this termination

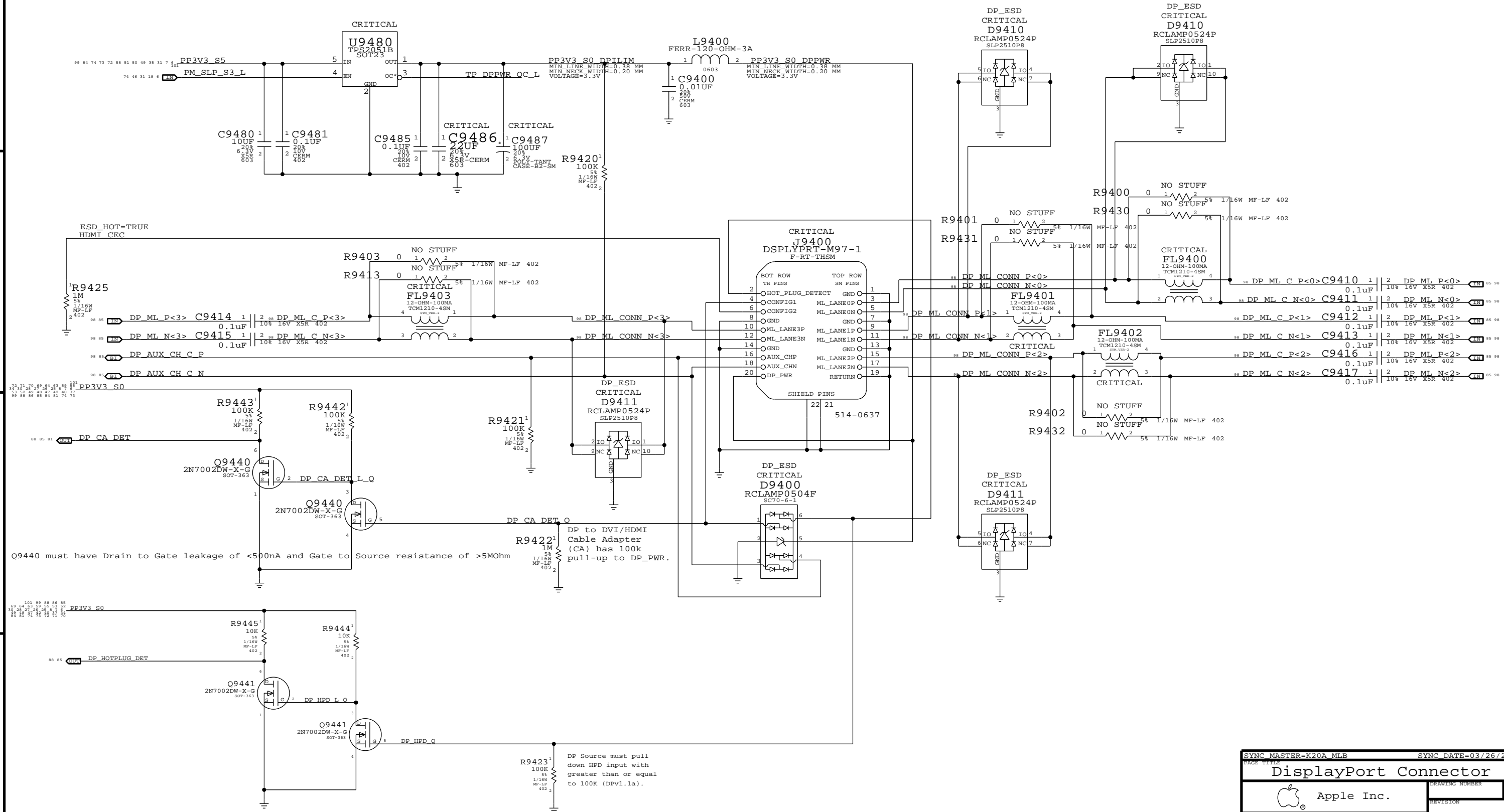



LVDS DDC MUX

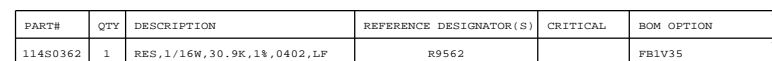


PAGE 1 OF 1		SYNC MASTER=K17 REF 114		SYNC DATE=06/17/2009	
Muxed Graphics Support					
		Apple Inc.		DRAWING NUMBER D	
				REVISION	
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Port Power Switch

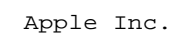


SYNC MASTER=K20A MLB		SYNC DATE=03/26/2009	
PAGE TITLE			
DisplayPort Connector			
 Apple Inc.		DRAWING NUMBER	
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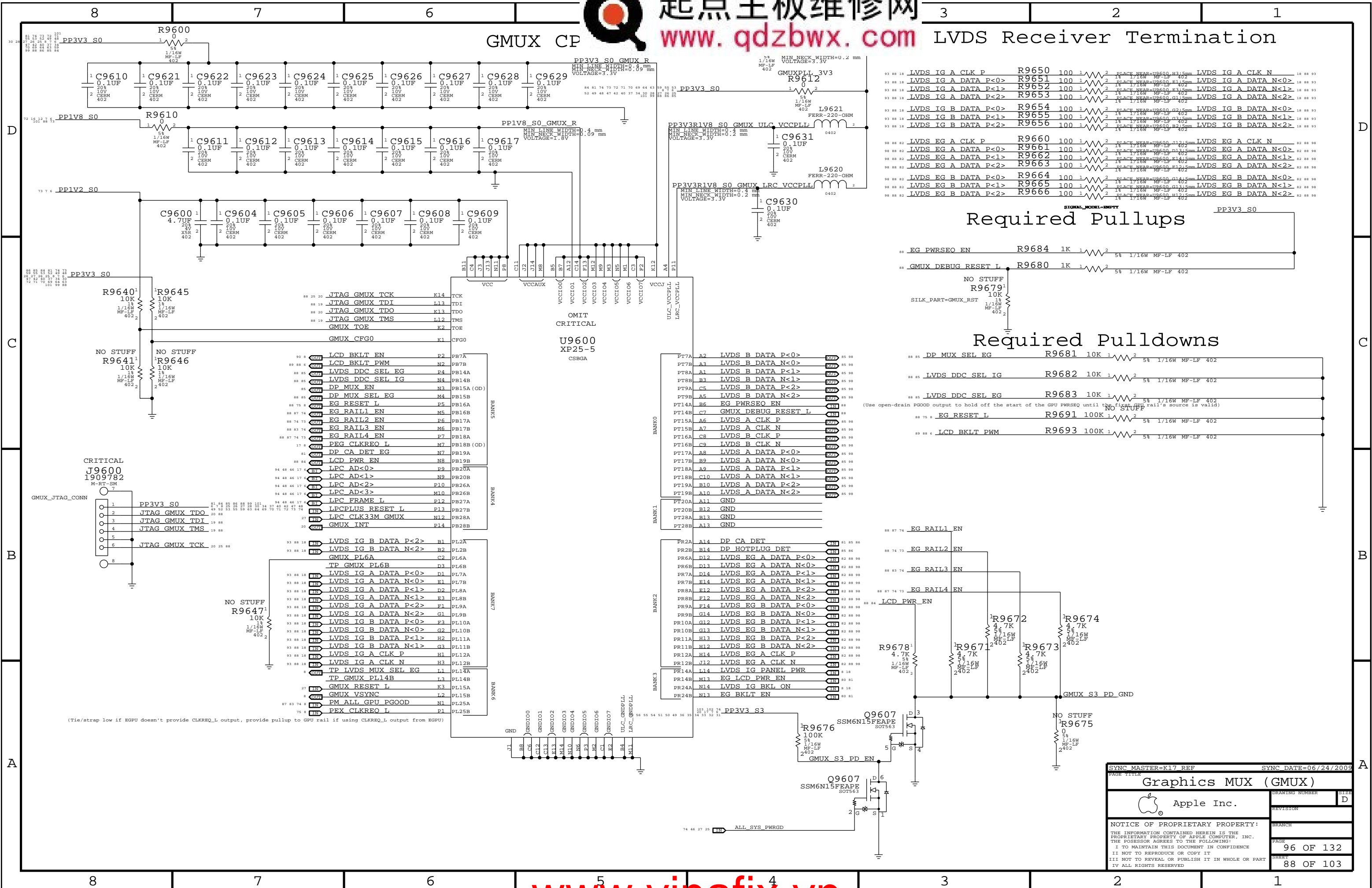



SYNC MASTER=K17 REF SYNC DATE=06/17/2009

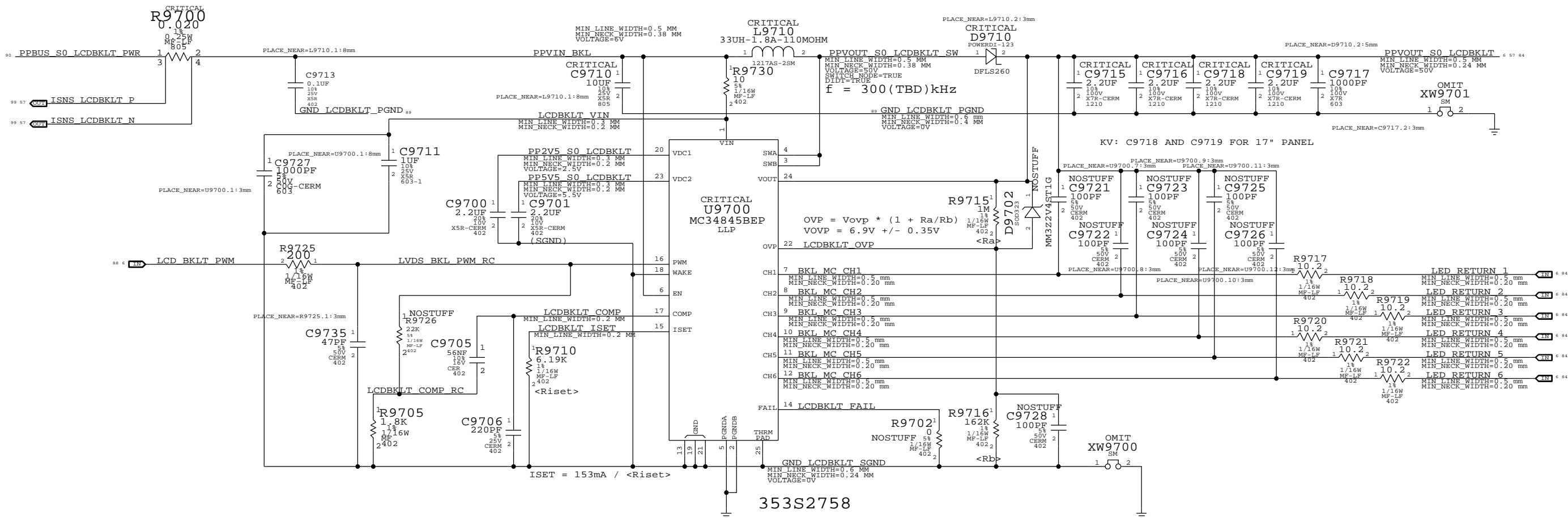
1.05V GPU / 1V8 FB Power Supply



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PAGE TITLE			
Graphics MUX (GMUX)			
 Apple Inc.		DRAWING NUMBER	SIZE D
		REVISION	
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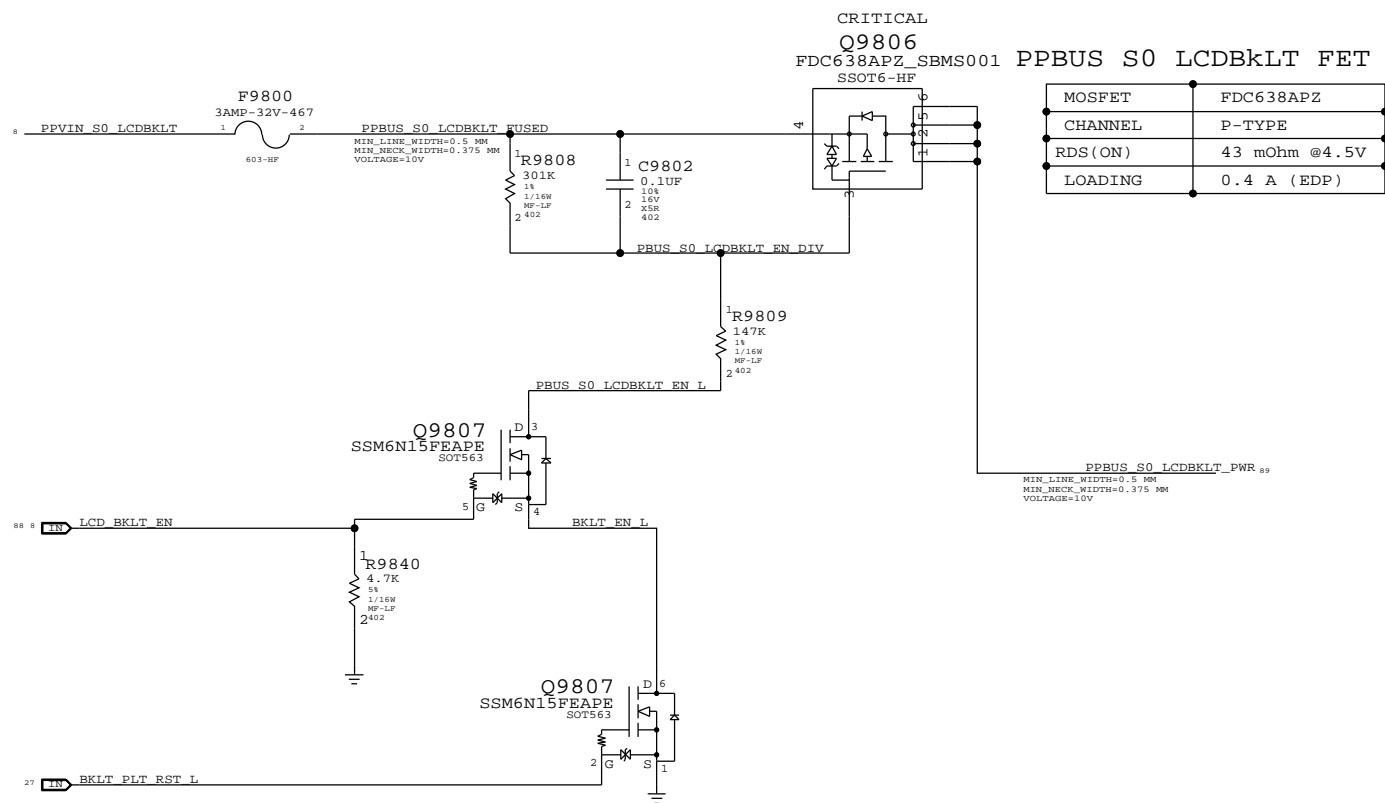
17 Inch Panel (14 LEDs per string)

Target: ISET = 25mA, OVP = 50V
ACTUAL: ISET = 24.7mA, OVP = 49.5V

KV: WAKE AND EN WIRING CHANGED FROM REF SCHEMATIC AS QFET IS PRESENT ON P.98

PLACEMENT_NOTE=PLACE XW9700 FAR FROM THE NOISY PINS 3 AND 4

SYNC MASTER=K17 VEMURI		SYNC DATE=12/16/2009	
PAGE TITLE			
LCD Backlight Driver (MC34845)			
 Apple Inc.	DRAWING NUMBER		SIZE
	REVISION		D
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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	20 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Calpella SFF DG (DG-407364_v1.5), Section 2.8

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.4

DMT_S2N	PCIE_85D	PCIE	DMI S2N P<3:0>	9 18
DMT_S2N	PCIE_85D	PCIE	DMI S2N N<3:0>	9 18
DMI_N2S	PCIE_85D	PCIE	DMI N2S P<3:0>	9 18
DMI_N2S	PCIE_85D	PCIE	DMI N2S N<3:0>	9 18
FDI_DATA	PCIE_85D	PCIE	FDI DATA P<7:0>	9 18
FDI_DATA	PCIE_85D	PCIE	FDI DATA N<7:0>	9 18
	CPU_50S	CPU_AGTL	FDI FSYNC<1..0>	9 18
	CPU_50S	CPU_AGTL	FDI LSYNC<1..0>	9 18
	CPU_50S	CPU_AGTL	FDI INT	9 18
CPU_PECT	CPU_50S	PCIE	CPU PECT	10 20
FSB_CPURST_L	CPU_50S	CPU_AGTL	FSB CPURST L	10 25
PM_SYNC	CPU_50S	CPU_AGTL	PM SYNC	10 18
PM_MEM_PWRGD	CPU_50S	CPU_AGTL	PM MEM PWRGD	10 18 31
CPU_VTT_S0_PGOOD	CPU_50S	CPU_AGTL	CPUVTT_S0_PGOOD	10 71
XDP_XPI_PWROOD	CPU_50S	CPU_ITP	XDP CPUPWRGD	10 25
XDP_DBRESET_L	CPU_50S	CPU_ITP	XDP DBRESET L	10 25 27
XDP_PRDY_L	CPU_50S	CPU_ITP	XDP PRDY L	10 25
XDP_PREQ_L	CPU_50S	CPU_ITP	XDP PREQ L	10 25
	CPU_50S	CPU_AGTL	PM EXT TS L<0>	10 47
	CPU_50S	CPU_AGTL	PM EXT TS L<1>	10 47
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU SM RCOMP0	10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU SM RCOMP1	10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU SM RCOMP2	10
CPU_CFG	CPU_50S	CPU_ITP	CPU CFG<17..0>	8 9 25
CPU_CATERR_L	CPU_50S	CPU_AGTL	CPU CATERR L	10
	CPU_50S	CPU_AGTL	TP CPU VTT SELECT	8 12
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU PROCHOT L	10 47 69
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU PWRGD	10 20 25
PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM THRMTRIP L	10 20 47
FSB_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	FSB CLK133M CPU_P	10 20
FSB_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	FSB CLK133M CPU_N	10 20
FSB_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	FSB CLK133M ITP_P	10 25
FSB_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	FSB CLK133M ITP_N	10 25
PCIE_CLK100M_CPU	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M CPU_P	10 17
PCIE_CLK100M_CPU	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M CPU_N	10 17
	CPU_55S	CPU_8MIL	CPU PSI L	12 15 69
PM_DPRSIPVR	CPU_50S	CPU_AGTL	PM DPRSLPVR	12 15 69
	CPU_27P4S	CPU_COMP	CPU PEG COMP	9
	CPU_27P4S	CPU_COMP	CPU PEG RBIAS	9
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP3	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP2	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP1	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP0	10
XDP_TDI	CPU_50S	CPU_ITP	XDP TDI	25
XDP_TDO	CPU_50S	CPU_ITP	XDP TDO	25
XDP_TMS	CPU_50S	CPU_ITP	XDP TMS	10 25
XDP_TCK	CPU_50S	CPU_ITP	XDP TCK	10 25
XDP_TEST_L	CPU_50S	CPU_ITP	XDP TRST L	10 25
XDP_BPM_L	CPU_50S	CPU_ITP	XDP BPM L<6..0>	10 25
XDP_BPM_L	CPU_50S	CPU_ITP	XDP BPM L<7>	10 25
(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP CPURST L	25
	CPU_55S	CPU_8MIL	CPU VID<6..0>	4 12 15
	CPU_50S	CPU_AGTL	CPUI MVP IMON	12 60 69
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE_P	12 69
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE_N	12 69
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VTTSENSE_P	12 71
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VTTSENSE_N	12 71
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	GFX VSENSE_P	13 70
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	GFX VSENSE_N	13 70
PM_DPRSIPVR	CPU_55S	CPU_8MIL	GFX VID<6..0>	8 13
	CPU_50S	CPU_AGTL	GFX DPRSLPVR	13 70
	CPU_50S	CPU_AGTL	GFX VR_EN	13 70
	CPU_50S	CPU_AGTL	GFXIMVP IMON	13 70
	PCIE_85D	PCIE	PEG R2D_P<15..0>	75
	PCIE_85D	PCIE	PEG R2D_N<15..0>	75
PEG_R2D	PCIE_85D	PCIE	PEG R2D_C_P<15..0>	8 75
	PCIE_85D	PCIE	PEG R2D_C_N<15..0>	8 75
PEG_D2R	PCIE_85D	PCIE	PEG D2R_P<15..0>	8 9 75
	PCIE_85D	PCIE	PEG D2R_N<15..0>	8 9 75
	PCIE_85D	PCIE	PEG D2R_C_P<15..0>	75
	PCIE_85D	PCIE	PEG D2R_C_N<15..0>	75



Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=3:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_20OTHER	*	25 MILS	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_20OTHER
MEM_CTRL	*	*	MEM_20OTHER
MEM_CMD	*	*	MEM_20OTHER
MEM_DATA	*	*	MEM_20OTHER
MEM_DQS	*	*	MEM_20OTHER

DDR3:

DQ/DM signals should be matched within 0.508mm of associated DQS pair.
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQS to clock matching should be within [CLK-12.7mm] and [CLK+25.4mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.
CONTROL signals should be matched within [CLK-12.7mm] to [CLK+0.0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-12.7mm] to [CLK+12.7mm] of CLK pairs.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to SODIMM pad is 139.7mm, from procesor ball to SODIMM pad is 114.3mm.

SOURCE: Calpella SFF Platform DG, Rev 1.5 (#407364), Section 2.2

MEM_A_CLK	MEM_72D	MEM_CLK	MEM A CLK P<5..0>	11 28
MEM_A_CLK	MEM_72D	MEM_CLK	MEM A CLK N<5..0>	11 28
MEM_A_CNTRL	MEM_37S	MEM_CTRL	MEM A CKE<3..0>	11 28
MEM_A_CNTRL	MEM_37S	MEM_CTRL	MEM A CS L<3..0>	11 28
MEM_A_CNTRL	MEM_37S	MEM_CTRL	MEM A ODT<3..0>	11 28
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A A<15..0>	11 28
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A BA<2..0>	11 28
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A RAS L	11 28
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A CAS L	11 28
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A WE L	11 28
MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM A DQ<7..0>	11 29
MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM A DQ<15..8>	11 29
MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM A DQ<23..16>	11 29
MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM A DQ<31..24>	11 29
MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM A DQ<39..32>	11 28 29
MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM A DQ<47..40>	11 29
MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM A DQ<55..48>	11 29
MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM A DQ<63..56>	11 29
MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM A DM<0>	11 28 29
MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM A DM<1>	11 29
MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM A DM<2>	11 29
MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM A DM<3>	11 29
MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM A DM<4>	11 29
MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM A DM<5>	11 29
MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM A DM<6>	11 29
MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM A DM<7>	11 29
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM A DQS P<0>	11 28 29
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM A DQS N<0>	11 28 29
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM A DQS P<1>	11 29
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM A DQS N<1>	11 29
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM A DQS P<2>	11 29
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM A DQS N<2>	11 29
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM A DQS P<3>	11 29
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM A DQS N<3>	11 29
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM A DQS P<4>	11 29
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM A DQS N<4>	11 29
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM A DQS P<5>	11 29
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM A DQS N<5>	11 29
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM A DQS P<6>	11 29
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM A DQS N<6>	11 29
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM A DQS P<7>	11 29
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM A DQS N<7>	11 29
MEM_B_CLK	MEM_72D	MEM_CLK	MEM B CLK P<5..0>	11 30
MEM_B_CLK	MEM_72D	MEM_CLK	MEM B CLK N<5..0>	11 30
MEM_B_CNTRL	MEM_37S	MEM_CTRL	MEM B CKE<3..0>	11 30
MEM_B_CNTRL	MEM_37S	MEM_CTRL	MEM B CS L<3..0>	11 30
MEM_B_CNTRL	MEM_37S	MEM_CTRL	MEM B ODT<3..0>	11 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B A<15..0>	11 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B BA<2..0>	11 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B RAS L	11 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B CAS L	11 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B WE L	11 30
MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM B DQ<7..0>	11 29
MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM B DQ<15..8>	11 29
MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM B DQ<23..16>	11 29
MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM B DQ<31..24>	11 29
MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM B DQ<39..32>	11 28 30
MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM B DQ<47..40>	11 29
MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM B DQ<55..48>	11 29
MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM B DQ<63..56>	11 29
MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM B DM<0>	11 29 30
MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM B DM<1>	11 29
MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM B DM<2>	11 29
MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM B DM<3>	11 29
MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM B DM<4>	11 29
MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM B DM<5>	11 29
MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM B DM<6>	11 29
MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM B DM<7>	11 29
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM B DQS P<0>	11 29 30
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM B DQS N<0>	11 29 30
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM B DQS P<1>	11 29
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM B DQS N<1>	11 29
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM B DQS P<2>	11 29
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM B DQS N<2>	11 29
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM B DQS P<3>	11 29
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM B DQS N<3>	11 29
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM B DQS P<4>	11 29
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM B DQS N<4>	11 29
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM B DQS P<5>	11 29
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM B DQS N<5>	11 29
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM B DQS P<6>	11 29
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM B DQS N<6>	11 29
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM B DQS P<7>	11 29
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM B DQS N<7>	11 29

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Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
LVDS_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?	DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?	LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length. DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps. DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals. Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?	SATA	TOP,BOTTOM	=3x_DIELECTRIC	?
SATA_ICOMP	*	8 MIL	?				

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

USB 2.0 Interface Constraints


PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?	USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.8

DP_ML	DP_85D	DISPLAYPORT	DP IG ML P<3..0>	8 85
DP_ML	DP_85D	DISPLAYPORT	DP IG ML N<3..0>	8 85
DP_AUX_CH	DP_85D	DISPLAYPORT	DP IG AUX_CH P	8 18 85
DP_AUX_CH	DP_85D	DISPLAYPORT	DP IG AUX_CH N	8 18 85
LVDS_IG_A_CLK	LVDS_85D	LVDS	LVDS IG A_CLK P	18 88
LVDS_IG_A_CLK	LVDS_85D	LVDS	LVDS IG A_CLK N	18 88
LVDS_IG_A_DATA	LVDS_85D	LVDS	LVDS IG A_DATA P<2..0>	18 88
LVDS_IG_A_DATA	LVDS_85D	LVDS	LVDS IG A_DATA N<2..0>	18 88
LVDS_IG_A_DATA3	LVDS_85D	LVDS	NC LVDS IG A_DATAP<3>	8 18
LVDS_IG_A_DATA3	LVDS_85D	LVDS	NC LVDS IG A_DATAN<3>	8 18
LVDS_IG_B_CLK	LVDS_85D	LVDS	TP LVDS IG B_CLKP	6 8 18
LVDS_IG_B_CLK	LVDS_85D	LVDS	TP LVDS IG B_CLKN	6 8 18
LVDS_IG_B_DATA	LVDS_85D	LVDS	LVDS IG B_DATA P<2..0>	18 88
LVDS_IG_B_DATA	LVDS_85D	LVDS	LVDS IG B_DATA N<2..0>	18 88
LVDS_IG_B_DATA3	LVDS_85D	LVDS	NC LVDS IG B_DATAP<3>	8 18
LVDS_IG_B_DATA3	LVDS_85D	LVDS	NC LVDS IG B_DATAN<3>	8 18
SATA_HDD_R2D	SATA_90D	SATA	SATA HDD R2D C P	17 42
SATA_90D	SATA		SATA HDD R2D C N	17 42
SATA_90D	SATA		SATA HDD R2D P	6 42
SATA_90D	SATA		SATA HDD R2D N	6 42
SATA_HDD_D2R	SATA_90D	SATA	SATA HDD D2R P	17 42
SATA_90D	SATA		SATA HDD D2R N	17 42
SATA_90D	SATA		SATA HDD D2R C P	42
SATA_90D	SATA		SATA HDD D2R C N	42
SATA_ODD_R2D	SATA_90D	SATA	SATA ODD R2D C P	17 42
SATA_90D	SATA		SATA ODD R2D C N	17 42
SATA_90D	SATA		SATA ODD R2D P	6 42
SATA_90D	SATA		SATA ODD R2D N	6 42
SATA_ODD_D2R	SATA_90D	SATA	SATA ODD D2R P	17 42
SATA_90D	SATA		SATA ODD D2R N	17 42
SATA_90D	SATA		SATA ODD D2R C P	42
SATA_90D	SATA		SATA ODD D2R C N	42
SATA_EXT_A_R2D	SATA_90D	SATA	TP SATA EXTA R2D C P	8 17
SATA_90D	SATA		TP SATA EXTA R2D C N	8 17
SATA_EXT_A_D2R	SATA_90D	SATA	TP SATA EXTA D2R P	8 17
SATA_90D	SATA		TP SATA EXTA D2R N	8 17
PCH_SATA_ICOMP		SATA_ICOMP	PCH SATA ICOMP	

USB_EXT_A	USB_85D	USB	USB_EXT_A P	36 43
USB_85D	USB		USB_EXT_A N	36 43
USB_EXT_B	USB_85D	USB	USB_EXT_B P	36 43
USB_85D	USB		USB_EXT_B N	36 43
USB_EXT_C	USB_85D	USB	USB_EXT_C P	35 44
USB_85D	USB		USB_EXT_C N	35 44
USB_HUB2_UP	USB_85D	USB	USB_HUB2 UP P	19 36
USB_85D	USB		USB_HUB2 UP N	19 36
USB_MINI	USB_85D	USB	NC USB MINIP	6
USB_85D	USB		NC USB MININ	6
USB_HUB1_UP	USB_85D	USB	USB_HUB1 UP P	19 35
USB_85D	USB		USB_HUB1 UP N	19 35
USB_CAMERA	USB_85D	USB	USB_CAMERA P	33 35
USB_85D	USB		USB_CAMERA N	33 35
USB_BT	USB_85D	USB	USB_BT P	33 36
USB_85D	USB		USB_BT N	33 36
USB_TPAD	USB_85D	USB	USB_TPAD P	36 54
USB_85D	USB		USB_TPAD N	36 54
USB_IR	USB_85D	USB	USB_IR P	35 45
USB_85D	USB		USB_IR N	35 45
USB_EXCARD	USB_85D	USB	USB_EXCARD P	8 34 36
USB_85D	USB		USB_EXCARD N	8 34 36
USB_BRCRYPT	USB_85D	USB	USB_BRCRYPT P	19 103
USB_85D	USB		USB_BRCRYPT N	19 103
PCH_USB_RBIAS	PCH_USB_RBIAS		PCH_USB_RBIAS	18
CLK_PCIE_90D	CLK_PCIE	PCIE	PCIE_CLK100M_PCH_P	17 26
CLK_PCIE_90D	CLK_PCIE		PCIE_CLK100M_PCH_N	17 26
CLK_PCIE_90D	CLK_PCIE	FSB	FSB_CLK133M_PCH_P	17 26
CLK_PCIE_90D	CLK_PCIE		FSB_CLK133M_PCH_N	17 26
CLK_PCIE_90D	CLK_PCIE	PCH	PCH_CLK96M_DOT_P	17 26
CLK_PCIE_90D	CLK_PCIE		PCH_CLK96M_DOT_N	17 26
CLK_PCIE_90D	CLK_PCIE	PCH	PCH_CLK100M_SATA_P	17 26
CLK_PCIE_90D	CLK_PCIE		PCH_CLK100M_SATA_N	17 26
CPU_50S	CLK_PCIE	PCH	PCH_CLK14P3M_REFCLK	17 26
CPU_50S	CLK_PCIE		PCH_CLK33M_PCIIIN	17 27
GFX_CLK_DPLLSS	CLK_PCIE_90D	CLK_PCIE	GFX_CLK120M_DPLLSS_P	10 17
GFX_CLK_DPLLSS	CLK_PCIE_90D	CLK_PCIE	GFX_CLK120M_DPLLSS_N	10 17

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8			7			6	
LPC Bus Constraints							
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD


SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

LPC_AD	LPC_50S	LPC	LPC_AD<3..0>	6 17 46 48 88
LPC_FRAME_L	LPC_50S	LPC	LPC_FRAME_L	6 17 46 48 88
LPC_RESET_L	LPC_50S	LPC	LPCPLUS_RESET_L	6 27 48 88
MCP_LPC_CLK0	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC_R	19 27
CLK_LPC_50S	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC	27 46
CLK_LPC_50S	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_LPCPLUS	6 27 48
SMBUS_PCH_CLK	SMB_50S	SMB	SMBUS_PCH_CLK	6 17 25 26 28 30 32 34 42 48 49
SMBUS_PCH_DATA	SMB_50S	SMB	SMBUS_PCH_DATA	64 17 25 26 28 30 32 34 42 48 49
SMBUS_PCH_0_CLK	SMB_50S	SMB	SML_PCH_0_CLK	17 49
SMBUS_PCH_0_DATA	SMB_50S	SMB	SML_PCH_0_DATA	17 49
SMBUS_PCH_1_CLK	SMB_50S	SMB	SML_PCH_1_CLK	17 49
SMBUS_PCH_1_DATA	SMB_50S	SMB	SML_PCH_1_DATA	17 49
HDA_BIT_CLK	HDA_50S	HDA	HDA_BIT_CLK	17 59
HDA_BIT_CLK_R	HDA_50S	HDA	HDA_BIT_CLK_R	17
HDA_SYNC	HDA_50S	HDA	HDA_SYNC	17 59
HDA_SYNC_R	HDA_50S	HDA	HDA_SYNC_R	17
HDA_RST_L	HDA_50S	HDA	HDA_RST_R_L	17
HDA_RST_L	HDA_50S	HDA	HDA_RST_L	17 59
HDA_SDIN0	HDA_50S	HDA	HDA_SDIN0	17 59
HDA_SDIN_CODEC	HDA_50S	HDA	HDA_SDIN_CODEC	17 59
HDA_SDOUT	HDA_50S	HDA	HDA_SDOUT	17 59
HDA_SDOUT_R	HDA_50S	HDA	HDA_SDOUT_R	17
PM_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK	18 47
SPI_CLK	SPI_55S	SPI	SPI_CLK_R	17 48
SPI_CLK	SPI_55S	SPI	SPI_CLK	48
SPI_MOST	SPI_55S	SPI	SPI_MOST_R	17 48
SPI_MOST	SPI_55S	SPI	SPI_MOST	48
SPI_MISO	SPI_55S	SPI	SPI_MISO	17 48
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	17 48
SPI_CS0	SPI_55S	SPI	SPI_CS0_L	48
PCIE_85D	PCIE	PCIE	PCIE_ENET_R2D_P	37
PCIE_85D	PCIE	PCIE	PCIE_ENET_R2D_N	37
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_C_P	17 37
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_C_N	17 37
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_P	17 37
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_N	17 37
PCIE_ENET_D2R_C_P	PCIE_85D	PCIE	PCIE_ENET_D2R_C_P	37
PCIE_ENET_D2R_C_N	PCIE_85D	PCIE	PCIE_ENET_D2R_C_N	37
PCIE_85D	PCIE	PCIE	PCIE_AP_R2D_P	6 33
PCIE_85D	PCIE	PCIE	PCIE_AP_R2D_N	6 33
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_C_P	17 33
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_C_N	17 33
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_P	6 17 33
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_N	6 17 33
PCIE_85D	PCIE	PCIE	PCIE_FW_R2D_P	39
PCIE_85D	PCIE	PCIE	PCIE_FW_R2D_N	39
PCIE_FW_R2D	PCIE_85D	PCIE	PCIE_FW_R2D_C_P	17 39
PCIE_FW_R2D	PCIE_85D	PCIE	PCIE_FW_R2D_C_N	17 39
PCIE_FW_D2R	PCIE_85D	PCIE	PCIE_FW_D2R_P	17 39
PCIE_FW_D2R	PCIE_85D	PCIE	PCIE_FW_D2R_N	17 39
PCIE_FW_D2R_C_P	PCIE_85D	PCIE	PCIE_FW_D2R_C_P	39
PCIE_FW_D2R_C_N	PCIE_85D	PCIE	PCIE_FW_D2R_C_N	39
PCIE_85D	PCIE	PCIE	PCIE_EXCARD_R2D_P	6 34
PCIE_85D	PCIE	PCIE	PCIE_EXCARD_R2D_N	6 34
PCIE_EXCARD_R2D	PCIE_85D	PCIE	PCIE_EXCARD_R2D_C_P	17 34
PCIE_EXCARD_R2D	PCIE_85D	PCIE	PCIE_EXCARD_R2D_C_N	17 34
PCIE_EXCARD_D2R	PCIE_85D	PCIE	PCIE_EXCARD_D2R_P	6 17 34
PCIE_EXCARD_D2R	PCIE_85D	PCIE	PCIE_EXCARD_D2R_N	6 17 34
MCP_PE0_REECLK	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_P	17 75
CLK_PCIE_90D	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_N	17 75
PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_P	17 37
CLK_PCIE_90D	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_N	17 37
MCP_PE1_REECLK	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_P	17 33
CLK_PCIE_90D	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_N	17 33
MCP_PE2_REECLK	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_P	17 39
CLK_PCIE_90D	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_N	17 39
MCP_PE3_REECLK	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	17 34
CLK_PCIE_90D	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	17 34
CPU_27B4S	CPU_COMP	CPU	PCH_VSS_NCTF<1>	6 20
CPU_27B4S	CPU_COMP	CPU	PCH_VSS_NCTF<2>	6 20
CPU_27B4S	CPU_COMP	CPU	PCH_VSS_NCTF<5>	6 20
CPU_27B4S	CPU_COMP	CPU	TP_PCH_VSS_NCTF<7>	20
CPU_27B4S	CPU_COMP	CPU	PCH_VSS_NCTF<9>	6 20 94
CPU_27B4S	CPU_COMP	CPU	PCH_VSS_NCTF<9>	6 20 94
CPU_27B4S	CPU_COMP	CPU	PCH_VSS_NCTF<11>	6 20
CPU_27B4S	CPU_COMP	CPU	PCH_VSS_NCTF<12>	6 20
CPU_27B4S	CPU_COMP	CPU	PCH_VSS_NCTF<15>	6 20
CPU_27B4S	CPU_COMP	CPU	PCH_VSS_NCTF<17>	6 20
CPU_27B4S	CPU_COMP	CPU	PCH_VSS_NCTF<19>	6 20
CPU_27B4S	CPU_COMP	CPU	PCH_VSS_NCTF<21>	6 20
CPU_27B4S	CPU_COMP	CPU	PCH_VSS_NCTF<22>	20
CPU_27B4S	CPU_COMP	CPU	PCH_VSS_NCTF<25>	6 20
CPU_27B4S	CPU_COMP	CPU	PCH_VSS_NCTF<27>	6 20
CPU_27B4S	CPU_COMP	CPU	PCH_VSS_NCTF<29>	6 20
PCIE_AP_D2R	PCIE_85D	PCIE	CONN_PCIE_AP_D2R_P	
PCIE_AP_D2R	PCIE_85D	PCIE	CONN_PCIE_AP_D2R_N	
PCIE_AP_R2D	PCIE_85D	PCIE	CONN_PCIE_AP_R2D_P	
PCIE_AP_R2D	PCIE_85D	PCIE	CONN_PCIE_AP_R2D_N	

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CAESAR II (Ethernet) Constraints								
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD	

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_3X	*	=3:1_SPACING	?

SOURCE: Broadcom 5764-DS04-RDS Page 38


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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	0.6 MM	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALI	27 37
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALO	27 37
	ENET_50S	ENET_3X	ENET_RESET_L	27 37
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<3..0>	37 38
	ENET_100D	ENET_MDI	ENET_MDI_N<3..0>	37 38


SYNC MASTER=K17 WFERRY		SYNC DATE=06/09/2009	
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Ethernet Constraints			
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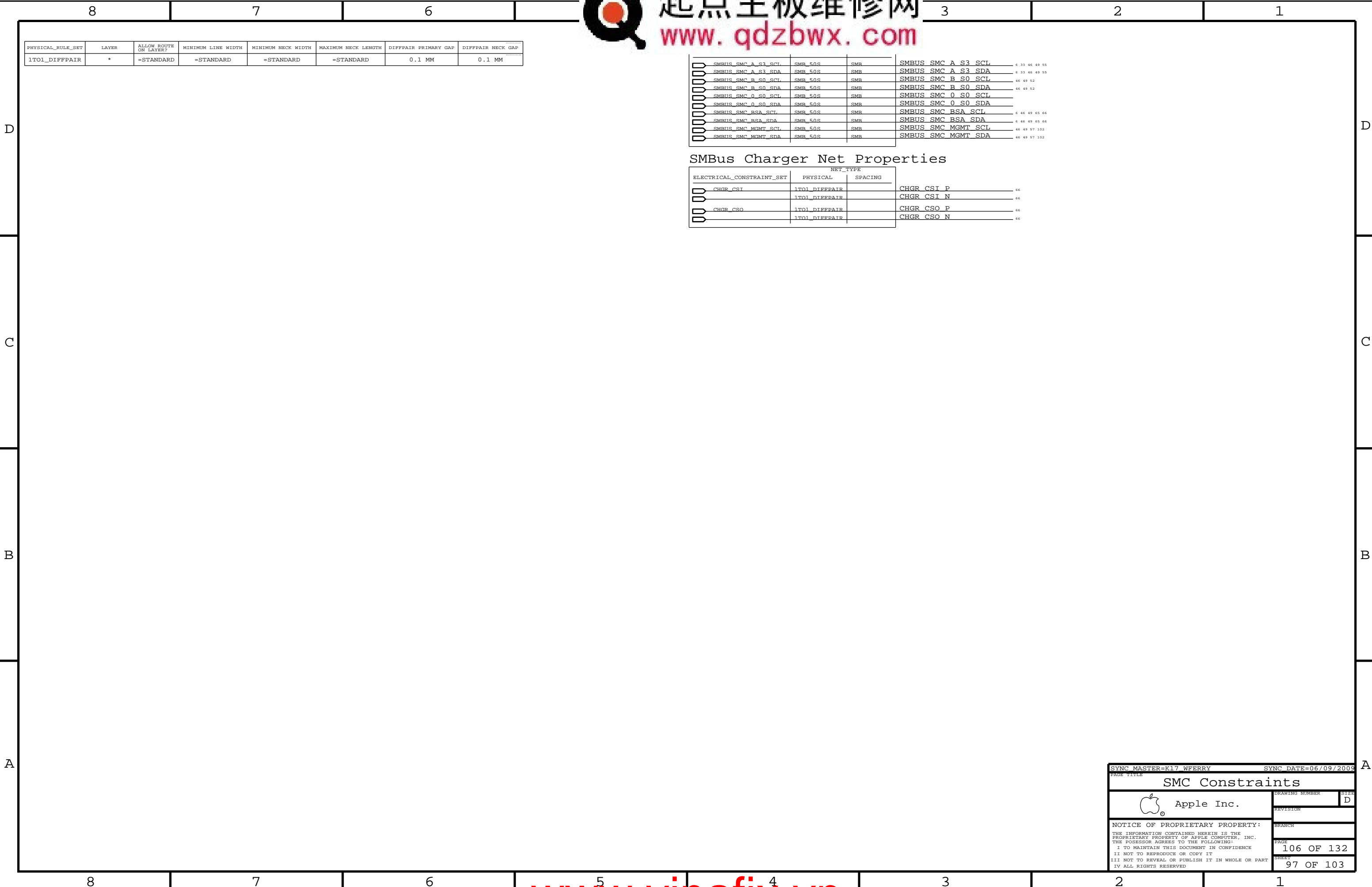


8			7			6			
FireWire Interface Constraints									
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF		

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

	FW_P0_TPA	FW_110D	FW_TP	NC FW0 TPAP	6 39 41
	FW_P0_TPB	FW_110D	FW_TP	NC FW0 TPAN	39 41
	FW_P0_TPB	FW_110D	FW_TP	NC FW0 TPBP	6 39 41
	FW_P0_TPB	FW_110D	FW_TP	NC FW0 TPBN	6 39 41
	FW_P1_TPA	FW_110D	FW_TP	FW PORT1 TPA P	39 40 41
	FW_P1_TPA	FW_110D	FW_TP	FW PORT1 TPA N	39 40 41
	FW_P1_TPB	FW_110D	FW_TP	FW PORT1 TPB P	39 40 41
	FW_P1_TPB	FW_110D	FW_TP	FW PORT1 TPB N	39 40 41
Port 2 Not Used					

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PAGE TITLE			
FireWire Constraints			
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PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

	SMBUS_SMC_A_S3_SCL	SMB_50S	SMB	SMBUS_SMC_A_S3_SCL	6 33 46 49 55
	SMBUS_SMC_A_S3_SDA	SMB_50S	SMB	SMBUS_SMC_A_S3_SDA	6 33 46 49 55
	SMBUS_SMC_B_S0_SCL	SMB_50S	SMB	SMBUS_SMC_B_S0_SCL	46 49 52
	SMBUS_SMC_B_S0_SDA	SMB_50S	SMB	SMBUS_SMC_B_S0_SDA	46 49 52
	SMBUS_SMC_0_S0_SCL	SMB_50S	SMB	SMBUS_SMC_0_S0_SCL	
	SMBUS_SMC_0_S0_SDA	SMB_50S	SMB	SMBUS_SMC_0_S0_SDA	
	SMBUS_SMC_BSA_SCL	SMB_50S	SMB	SMBUS_SMC_BSA_SCL	6 46 49 65 66
	SMBUS_SMC_BSA_SDA	SMB_50S	SMB	SMBUS_SMC_BSA_SDA	6 46 49 65 66
	SMBUS_SMC_MGMT_SCL	SMB_50S	SMB	SMBUS_SMC_MGMT_SCL	46 49 57 102
	SMBUS_SMC_MGMT_SDA	SMB_50S	SMB	SMBUS_SMC_MGMT_SDA	46 49 57 102

SMBus Charger Net Properties

NET_TYPE		
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING
	CHGR_CSI	1TO1_DIFFPAIR
	CHGR_CSI	1TO1_DIFFPAIR
	CHGR_CSI	1TO1_DIFFPAIR
	CHGR_CSI	1TO1_DIFFPAIR

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SMC Constraints

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8		7		6			
GDDR3 Frame Buffer Signal Constraints							
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR3_40R55SE	*	=55_OHM_SE	=40_OHM_SE	0.095 MM	12.7 MM	=STANDARD	=STANDARD
GDDR3_40SE	*	=40_OHM_SE	=40_OHM_SE	0.095 MM	=40_OHM_SE	=STANDARD	=STANDARD
GDDR3_80D	*	=85_OHM_DIFF	=85_OHM_DIFF	0.095 MM	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR3_CLK	*	=2.5:1_SPACING	?
GDDR3_CMD	*	=2.5:1_SPACING	?
GDDR3_DATA	*	=2.5:1_SPACING	?
GDDR3_DQS	*	=2.5:1_SPACING	?

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
LVDS_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?	DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?	LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 0.127 mm. Pairs should be within 0.508mm of entire channel.
DisplayPort/TMDS intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.
DisplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.
Max length of LVDS/DisplayPort/TMDS traces: 13 inches.
SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.

MUXGFX Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE	
PHYSICAL	SPACING		
LVDS_A_CLK	LVDS_85D	LVDS	LVDS A CLK P
LVDS_A_CLK	LVDS_85D	LVDS	LVDS A CLK N
LVDS_A_DATA	LVDS_85D	LVDS	LVDS A DATA P<2..0>
LVDS_A_DATA	LVDS_85D	LVDS	LVDS A DATA N<2..0>
LVDS_B_CLK	LVDS_85D	LVDS	LVDS B CLK P
LVDS_B_CLK	LVDS_85D	LVDS	LVDS B CLK N
LVDS_B_DATA	LVDS_85D	LVDS	LVDS B DATA P<2..0>
LVDS_B_DATA	LVDS_85D	LVDS	LVDS B DATA N<2..0>
LVDS_CONN_A_CLK_F_P	LVDS_85D	LVDS	LVDS CONN A CLK F P
LVDS_CONN_A_CLK_F_N	LVDS_85D	LVDS	LVDS CONN A CLK F N
LVDS_CONN_B_CLK_F_P	LVDS_85D	LVDS	LVDS CONN B CLK F P
LVDS_CONN_B_CLK_F_N	LVDS_85D	LVDS	LVDS CONN B CLK F N
LVDS_CONN_A_CLK_P	LVDS_85D	LVDS	LVDS CONN A CLK P
LVDS_CONN_A_CLK_N	LVDS_85D	LVDS	LVDS CONN A CLK N
LVDS_CONN_A_DATA_P<2..0>	LVDS_85D	LVDS	LVDS CONN A DATA P<2..0>
LVDS_CONN_A_DATA_N<2..0>	LVDS_85D	LVDS	LVDS CONN A DATA N<2..0>
LVDS_CONN_B_CLK_P	LVDS_85D	LVDS	LVDS CONN B CLK P
LVDS_CONN_B_CLK_N	LVDS_85D	LVDS	LVDS CONN B CLK N
LVDS_CONN_B_DATA_P<2..0>	LVDS_85D	LVDS	LVDS CONN B DATA P<2..0>
LVDS_CONN_B_DATA_N<2..0>	LVDS_85D	LVDS	LVDS CONN B DATA N<2..0>
DP_ML	DP_85D	DISPLAYPORT	DP ML C P<3..0>
DP_ML	DP_85D	DISPLAYPORT	DP ML C N<3..0>
DP_ML	DP_85D	DISPLAYPORT	DP ML P<3..0>
DP_ML	DP_85D	DISPLAYPORT	DP ML N<3..0>
DP_ML	DP_85D	DISPLAYPORT	DP ML CONN P<3..0>
DP_ML	DP_85D	DISPLAYPORT	DP ML CONN N<3..0>
DP_AUX_CH	DP_85D	DISPLAYPORT	DP AUX CH C P
DP_AUX_CH	DP_85D	DISPLAYPORT	DP AUX CH C N

GDDR3 1

ELECTRICAL_CONSTRAINT_SET		NET_TYPE	
PHYSICAL	SPACING		
FB_A_CLK	GDDR3_80D	GDDR3_CLK	FB A CLK P<0>
FB_A_CLK	GDDR3_80D	GDDR3_CLK	FB A CLK N<0>
FB_B_CLK	GDDR3_80D	GDDR3_CLK	FB A CLK P<1>
FB_B_CLK	GDDR3_80D	GDDR3_CLK	FB A CLK N<1>
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB A MA<1..0>
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB A MA<12..6>
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB A BA<2..0>
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB A RAS L
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB A CAS L
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB A WE L
FB_AB_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB A UCKE
FB_AB_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB A LCKE
FB_AB_CS0	GDDR3_40R55SE	GDDR3_CMD	FB A LCS0 L
FB_AB_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB A DRAM RST
FB_A_CMD	GDDR3_40SE	GDDR3_CMD	FB A LMA<5..2>
FB_B_CMD	GDDR3_40SE	GDDR3_CMD	FB A UMA<5..2>
FB_A_WDQS0	GDDR3_40SE	GDDR3_DQS	FB A WDQS<0>
FB_A_WDQS1	GDDR3_40SE	GDDR3_DQS	FB A WDQS<1>
FB_A_WDQS2	GDDR3_40SE	GDDR3_DQS	FB A WDQS<2>
FB_A_WDQS3	GDDR3_40SE	GDDR3_DQS	FB A WDQS<3>
FB_A_RDQS0	GDDR3_40SE	GDDR3_DQS	FB A RDQS<0>
FB_A_RDQS1	GDDR3_40SE	GDDR3_DQS	FB A RDQS<1>
FB_A_RDQS2	GDDR3_40SE	GDDR3_DQS	FB A RDQS<2>
FB_A_RDQS3	GDDR3_40SE	GDDR3_DQS	FB A RDQS<3>
FB_A_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB A DQ<7..0>
FB_A_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB A DQ<15..8>
FB_A_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB A DQ<23..16>
FB_A_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB A DQ<31..24>
FB_A_DQM0	GDDR3_40SE	GDDR3_DATA	FB A DQM L<0>
FB_A_DQM1	GDDR3_40SE	GDDR3_DATA	FB A DQM L<1>
FB_A_DQM2	GDDR3_40SE	GDDR3_DATA	FB A DQM L<2>
FB_A_DQM3	GDDR3_40SE	GDDR3_DATA	FB A DQM L<3>
FB_B_WDQS0	GDDR3_40SE	GDDR3_DQS	FB A WDQS<4>
FB_B_WDQS1	GDDR3_40SE	GDDR3_DQS	FB A WDQS<5>
FB_B_WDQS2	GDDR3_40SE	GDDR3_DQS	FB A WDQS<6>
FB_B_WDQS3	GDDR3_40SE	GDDR3_DQS	FB A WDQS<7>
FB_B_RDQS0	GDDR3_40SE	GDDR3_DQS	FB A RDQS<4>
FB_B_RDQS1	GDDR3_40SE	GDDR3_DQS	FB A RDQS<5>
FB_B_RDQS2	GDDR3_40SE	GDDR3_DQS	FB A RDQS<6>
FB_B_RDQS3	GDDR3_40SE	GDDR3_DQS	FB A RDQS<7>
FB_B_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB A DQ<39..32>
FB_B_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB A DQ<47..40>
FB_B_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB A DQ<55..48>
FB_B_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB A DQ<63..56>
FB_B_DQM0	GDDR3_40SE	GDDR3_DATA	FB A DQM L<4>
FB_B_DQM1	GDDR3_40SE	GDDR3_DATA	FB A DQM L<5>
FB_B_DQM2	GDDR3_40SE	GDDR3_DATA	FB A DQM L<6>
FB_B_DQM3	GDDR3_40SE	GDDR3_DATA	FB A DQM L<7>

G96 Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE	
PHYSICAL	SPACING		
CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M	
CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M_SS	
LVDS_EG_A_CLK	LVDS_85D	LVDS EG A CLK P	
LVDS_EG_A_CLK	LVDS_85D	LVDS EG A CLK N	
LVDS_EG_A_DATA	LVDS_85D	LVDS EG A DATA P<2..0>	
LVDS_EG_A_DATA	LVDS_85D	LVDS EG A DATA N<2..0>	
LVDS_EG_A_DATA3	LVDS_85D	NC LVDS EG A DATA P<3>	
LVDS_EG_A_DATA3	LVDS_85D	NC LVDS EG A DATA N<3>	
LVDS_EG_B_DATA	LVDS_85D	LVDS EG B DATA P<2..0>	
LVDS_EG_B_DATA	LVDS_85D	LVDS EG B DATA N<2..0>	
LVDS_EG_B_DATA3	LVDS_85D	NC LVDS EG B DATA P<3>	
LVDS_EG_B_DATA3	LVDS_85D	NC LVDS EG B DATA N<3>	
DP_ML	DP_85D	DP EG ML P<3..0>	
DP_ML	DP_85D	DP EG ML N<3..0>	
DP_AUX_CH	DP_85D	DP EG AUX CH P	
DP_AUX_CH	DP_85D	DP EG AUX CH N	
DP_AUX_CH	DP_85D	DP EG AUX CH C P	
DP_AUX_CH	DP_85D	DP EG AUX CH C N	

GDDR3 FB C/D Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE	
PHYSICAL	SPACING		
FB_C_CLK	GDDR3_80D	GDDR3_CLK	FB B CLK P<0>
FB_C_CLK	GDDR3_80D	GDDR3_CLK	FB B CLK N<0>
FB_D_CLK	GDDR3_80D	GDDR3_CLK	FB B CLK P<1>
FB_D_CLK	GDDR3_80D	GDDR3_CLK	FB B CLK N<1>
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB B MA<1..0>
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB B MA<12..6>
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB B BA<2..0>
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB B RAS L
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB B CAS L
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB B WE L
FB_CD_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB B UCKE
FB_CD_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB B LCKE
FB_CD_CS0	GDDR3_40R55SE	GDDR3_CMD	FB B LCS0 L
FB_CD_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB B DRAM RST
FB_C_CMD	GDDR3_40SE	GDDR3_CMD	FB B LMA<5..2>
FB_D_CMD	GDDR3_40SE	GDDR3_CMD	FB B UMA<5..2>
FB_C_WDQS0	GDDR3_40SE	GDDR3_DQS	FB B WDQS<0>
FB_C_WDQS1	GDDR3_40SE	GDDR3_DQS	FB B WDQS<1>
FB_C_WDQS2	GDDR3_40SE	GDDR3_DQS	FB B WDQS<2>
FB_C_WDQS3	GDDR3_40SE	GDDR3_DQS	FB B WDQS<3>
FB_C_RDQS0	GDDR3_40SE	GDDR3_DQS	FB B RDQS<0>
FB_C_RDQS1	GDDR3_40SE	GDDR3_DQS	FB B RDQS<1>
FB_C_RDQS2	GDDR3_40SE	GDDR3_DQS	FB B RDQS<2>
FB_C_RDQS3	GDDR3_40SE	GDDR3_DQS	FB B RDQS<3>
FB_C_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB B DQ<7..0>
FB_C_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB B DQ<15..8>
FB_C_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB B DQ<23..16>
FB_C_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB B DQ<31..24>
FB_C_DQM0	GDDR3_40SE	GDDR3_DATA	FB B DQM L<0>
FB_C_DQM1	GDDR3_40SE	GDDR3_DATA	FB B DQM L<1>
FB_C_DQM2	GDDR3_40SE	GDDR3_DATA	FB B DQM L<2>
FB_C_DQM3	GDDR3_40SE	GDDR3_DATA	FB B DQM L<3>
FB_D_WDQS0	GDDR3_40SE	GDDR3_DQS	FB B WDQS<4>
FB_D_WDQS1	GDDR3_40SE	GDDR3_DQS	FB B WDQS<5>
FB_D_WDQS2	GDDR3_40SE	GDDR3_DQS	FB B WDQS<6>
FB_D_WDQS3	GDDR3_40SE	GDDR3_DQS	FB B WDQS<7>
FB_D_RDQS0	GDDR3_40SE	GDDR3_DQS	FB B RDQS<4>
FB_D_RDQS1	GDDR3_40SE	GDDR3_DQS	FB B RDQS<5>
FB_D_RDQS2	GDDR3_40SE	GDDR3_DQS	FB B RDQS<6>
FB_D_RDQS3	GDDR3_40SE	GDDR3_DQS	FB B RDQS<7>
FB_D_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB B DQ<39..32>
FB_D_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB B DQ<47..40>
FB_D_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB B DQ<55..48>
FB_D_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB B DQ<63..56>
FB_D_DQM0	GDDR3_40SE	GDDR3_DATA	FB B DQM L<4>
FB_D_DQM1	GDDR3_40SE	GDDR3_DATA	FB B DQM L<5>
FB_D_DQM2	GDDR3_40SE	GDDR3_DATA	FB B DQM L<6>
FB_D_DQM3	GDDR3_40SE	GDDR3_DATA	FB B DQM L<7>

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GPU (GT216) CONSTRAINTS					
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8		7			6		
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_I101_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_I101_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	+	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCI_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
USB_85D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	BOTTOM OVERRIDE	OVERRIDE	OVERRIDE	0.23 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_85D	BGA	LVDS_85D
DP_85D	BGA	100_DIFF_BGA
SATA_90D	BGA	100_DIFF_BGA
CLK_PCIE_90D	BGA	100_DIFF_BGA


PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFFAIR PRIMARY GAP	DIFFFAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

K17 S1

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING			
	ENET 100D	ENETCONN	ENETCONN P<3...0>	38	
	ENET 100D	ENETCONN	ENETCONN N<3...0>	38	
	SATA 90D	SATA	SATA ODD R2D UF P	42	
	SATA 90D	SATA	SATA ODD R2D UF N	42	
	SATA 90D	SATA	SATA ODD D2R UF P	42	
	SATA 90D	SATA	SATA ODD D2R UF N	42	
	SATA 90D	SATA	SATA HDD D2R UF P	42	
	SATA 90D	SATA	SATA HDD D2R UF N	42	
	SATA 90D	SATA	SATA HDD R2D UF P	42	
	SATA 90D	SATA	SATA HDD R2D UF N	42	
	SATA 90D	SATA	SATA HDD D2R EDRV IN P	42	
	SATA 90D	SATA	SATA HDD D2R EDRV IN N	42	
	SATA 90D	SATA	SATA HDD D2R EDRV OUT P	42	
	SATA 90D	SATA	SATA HDD D2R EDRV OUT N	42	
	SATA 90D	SATA	SATA HDD R2D EDRV IN P	42	
	SATA 90D	SATA	SATA HDD R2D EDRV IN N	42	
	SATA 90D	SATA	SATA HDD R2D EDRV OUT P	42	
	SATA 90D	SATA	SATA HDD R2D EDRV OUT N	42	
	SENSE DIFFPAIR	THERM 1701 55G	THERM	CPUTHMSNS D2 P	52
	SENSE DIFFPAIR	THERM 1701 55G	THERM	CPUTHMSNS D2 N	52
	SENSE DIFFPAIR	THERM 1701 55G	THERM	CPU THERMD P	52
	SENSE DIFFPAIR	THERM 1701 55G	THERM	CPU THERMD N	52
	SENSE DIFFPAIR	THERM 1701 55G	THERM	GPUTHMSNS D P	52
	SENSE DIFFPAIR	THERM 1701 55G	THERM	GPUTHMSNS D N	52
	SENSE DIFFPAIR	THERM 1701 55G	THERM	GPU TDIODE P	52
	SENSE DIFFPAIR	THERM 1701 55G	THERM	GPU TDIODE N	52
	SENSE DIFFPAIR	SENSE 1701 55G	THERM	ISNS 3V3 S3 R P	102
	SENSE DIFFPAIR	SENSE 1701 55G	THERM	ISNS 3V3 S3 R N	102
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	ISNS AIRPORT P	13
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	ISNS AIRPORT N	13
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	DDRISNS R P	67
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	DDRISNS R N	67
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	GPUISNS P	51
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	GPUISNS N	51
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	ISNS AIRPORT P	13
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	ISNS AIRPORT N	13
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	DDRISNS P	67
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	DDRISNS N	67
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	ISNS P1V8GPU P	51
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	ISNS P1V8GPU N	51
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	ISNS CPU P	40
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	ISNS CPU N	40
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	ISNS P1V8GPU R P	61
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	ISNS P1V8GPU R N	61
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	ISNS HDD P	42
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	ISNS HDD N	42
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	ISNS HDD R P	57
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	ISNS HDD R N	57
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	ISNS ODD R P	57
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	ISNS ODD R N	57
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	ISNS ODD P	42
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	ISNS ODD N	42
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	ISNS LCBKILT P	67
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	ISNS LCBKILT N	67
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	NC ISNS P1V05S0PCH P	8
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	NC ISNS P1V05S0PCH N	8
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	CPUVTT50 CS P	71
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	CPUVTT50 CS N	71
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	CPUVTT50 CS R P	71
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	CPUVTT50 CS R N	71
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	NC ISNS P3V1S0MPCH P	8
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	NC ISNS P3V1S0MPCH N	8
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	ISNS P3V1S0MPCH R P	102
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	ISNS P3V1S0MPCH R N	102
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	GFIXIMVP CS P	70
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	GFIXIMVP CS N	70
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	GFIXIMVP CS R P	60
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	GFIXIMVP CS R N	60
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	ISNS PP5V S0 R P	102
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	ISNS PP5V S0 R N	102
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	NC ISNS PVTTS0PCH P	8
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	NC ISNS PVTTS0PCH N	8
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	ISNS PVTTS0PCH R P	102
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	ISNS PVTTS0PCH R N	102
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	ISNS PP1V05 P	51
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	ISNS PP1V05 N	51
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	ISNS PP3V3 S3 P	102
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	ISNS PP3V3 S3 N	102
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	ISNS PP3V3 S5 P	61
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	ISNS PP3V3 S5 N	61
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	ISNS PP5V S0 P	102
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	ISNS PP5V S0 N	102
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	ISNS PP5V S3 P	51
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	ISNS PP5V S3 N	51
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	ISNS LV5 S3 P	51
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	ISNS LV5 S3 N	51
	SENSE DIFFPAIR	SENSE 1701 55G	THERM	ISNS LV5 S3 R P	51
	SENSE DIFFPAIR	SENSE 1701 55G	THERM	ISNS LV5 S3 R N	51
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	ISNS AIRPORT R P	67
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	ISNS AIRPORT R N	67
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	GFIXIMVP6 VSEN P	63
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	GFIXIMVP6 VSEN N	63
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	GFIX ISNS R P	50
	SENSE DIFFPAIR	SENSE 1701 55G	SENSE	GFIX ISNS R N	50

K17 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	
PCIE CLK100M AP	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M AP CONN P 6 33
	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M AP CONN N 6 33
	1T01_DIEFFPAIR		CHGR CSI R P 66
	1T01_DIEFFPAIR		CHGR CSI R N 66
	1T01_DIEFFPAIR		CHGR CSO R P 50 66
	1T01_DIEFFPAIR		CHGR CSO R N 50 66
(USB_EXT_A)	USB_R5D	USB	USB2 EXTA MIXED P 43
(USB_EXT_A)	USB_R5D	USB	USB2 EXTA MIXED N 43
(USB_EXT_A)	USB_R5D	USB	USB2 LT1 P 6 43
(USB_EXT_A)	USB_R5D	USB	USB2 LT1 N 6 43
(USB_EXTD)	USB_R5D	USB	USB BRCRYPT CONN P
(USB_EXTD)	USB_R5D	USB	USB BRCRYPT CONN N
(USB_CAMERA)	USB_R5D	USB	USB CAMERA CONN P 6 33
(USB_CAMERA)	USB_R5D	USB	USB CAMERA CONN N 6 33
	USB_R5D	USB	CONN USB2 BT P 6 33
	USB_R5D	USB	CONN USB2 BT N 6 33
	USB_R5D	USB	USB LT2 P 6 43
	USB_R5D	USB	USB LT2 N 6 43
	USB_R5D	USB	USB2 EXCARD CONN P 6 34
	USB_R5D	USB	USB2 EXCARD CONN N 6 34
DP_85D	DISPLAYPORT		DP IG AUX CH C P 85
DP_85D	DISPLAYPORT		DP IG AUX CH C N 85
USB_R5D	USB		USB BRCRYPT R P
USB_R5D	USB		USB BRCRYPT R N
CLK_PCIE_90D	CLK_PCIE		PCIE CLK100M EXCARD CONN N 6 34
CLK_PCIE_90D	CLK_PCIE		PCIE CLK100M EXCARD CONN P 6 34
SPK_OUT	DIEFFPAIR	AUDIO	SPKRAMP FL OUT P 6 62 63
	DIEFFPAIR	AUDIO	SPKRAMP FL OUT N 6 62 63
SPK_OUT	DIEFFPAIR	AUDIO	SPKRAMP BL OUT P 6 62 63
	DIEFFPAIR	AUDIO	SPKRAMP BL OUT N 6 62 63
SPK_OUT	DIEFFPAIR	AUDIO	SPKRAMP FR OUT P 6 62 63
	DIEFFPAIR	AUDIO	SPKRAMP FR OUT N 6 62 63
SPK_OUT	DIEFFPAIR	AUDIO	SPKRAMP BR OUT P 6 62 63
	DIEFFPAIR	AUDIO	SPKRAMP BR OUT N 6 62 63
SPK_OUT	DIEFFPAIR	AUDIO	SPKRAMP LFE OUT P 6 62 63
	DIEFFPAIR	AUDIO	SPKRAMP LFE OUT N 6 62 63
USB_R5D	DIEFFPAIR	AUDIO	SPKRAMP FL IN C P 62
USB_R5D	DIEFFPAIR	AUDIO	SPKRAMP FL IN C N 62
USB_R5D	DIEFFPAIR	AUDIO	SPKRAMP BL IN C P 62
USB_R5D	DIEFFPAIR	AUDIO	SPKRAMP BL IN C N 62
USB_R5D	DIEFFPAIR	AUDIO	SPKRAMP FR IN C P 62
USB_R5D	DIEFFPAIR	AUDIO	SPKRAMP FR IN C N 62
USB_R5D	DIEFFPAIR	AUDIO	SPKRAMP BR IN C P 62
USB_R5D	DIEFFPAIR	AUDIO	SPKRAMP BR IN C N 62
USB_R5D	DIEFFPAIR	AUDIO	SPKRAMP LFE IN C P 62
USB_R5D	DIEFFPAIR	AUDIO	SPKRAMP LFE IN C N 62
USB_R5D	DIEFFPAIR	AUDIO	SPKRAMP FL IN L P 62
USB_R5D	DIEFFPAIR	AUDIO	SPKRAMP FL IN L N 62
USB_R5D	DIEFFPAIR	AUDIO	SPKRAMP BL IN L P 62
USB_R5D	DIEFFPAIR	AUDIO	SPKRAMP BL IN L N 62
USB_R5D	DIEFFPAIR	AUDIO	SPKRAMP FR IN L P 62
USB_R5D	DIEFFPAIR	AUDIO	SPKRAMP FR IN L N 62
USB_R5D	DIEFFPAIR	AUDIO	SPKRAMP BR IN L P 62
USB_R5D	DIEFFPAIR	AUDIO	SPKRAMP BR IN L N 62
USB_R5D	DIEFFPAIR	AUDIO	SPKRAMP LFE IN L P 62
USB_R5D	DIEFFPAIR	AUDIO	SPKRAMP LFE IN L N 62
USB_R5D	DIEFFPAIR	AUDIO	SSM2315FL IN P 62
USB_R5D	DIEFFPAIR	AUDIO	SSM2315FL IN N 62
USB_R5D	DIEFFPAIR	AUDIO	SSM2315FR IN P 62
USB_R5D	DIEFFPAIR	AUDIO	SSM2315FR IN N 62
USB_R5D	DIEFFPAIR	AUDIO	SSM2315BR IN P 62
USB_R5D	DIEFFPAIR	AUDIO	SSM2315BR IN N 62
USB_R5D	DIEFFPAIR	AUDIO	INT MIC F P 6 63 64
USB_R5D	DIEFFPAIR	AUDIO	INT MIC F N 6 63 64
USB_R5D	DIEFFPAIR	AUDIO	INT MIC P 6 63
USB_R5D	DIEFFPAIR	AUDIO	INT MIC N 6 63
USB_R5D	DIEFFPAIR	AUDIO	SSM2315BL IN P 62
USB_R5D	DIEFFPAIR	AUDIO	SSM2315BL IN N 62
USB_R5D	DIEFFPAIR	AUDIO	SSM2315LFE IN P 62
USB_R5D	DIEFFPAIR	AUDIO	SSM2315LFE IN N 62
USB_R5D	USB		USB TPAD R P 54
USB_R5D	USB		USB TPAD R N 54
USB_R5D	USB		USB LT3 P 6 44
USB_R5D	USB		USB LT3 N 6 44
	SR_POWER		PP3V3_S5 84, 85, 101
	SR_POWER		PP3V3_S0 69, 70, 71, 72
	SR_POWER		PP1V5_S0 42, 43, 44, 45
	GND		GND 88, 101 34, 42, 59

SYNC MASTER=K17 REF		SYNC DATE=06/17/2009	
PAGE TITLE			
Project Specific Constraints			
 Apple Inc.		DRAWING NUMBER	SIZE
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K17 Board-Specific Spacing & Physical Constraints

BOARD LAYERS				BOARD AREAS		BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM				NO_TYPE, BGA		MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP, BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.110 MM	0.095 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP, BOTTOM	Y	0.185 MM	0.095 MM			
37_OHM_SE	*	Y	0.155 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP, BOTTOM	Y	0.310 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.250 MM	0.250 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP, BOTTOM	Y	0.165 MM	0.095 MM			
40_OHM_SE	*	Y	0.135 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3, ISL4	Y	0.154 MM	0.154 MM		0.200 MM	0.200 MM
72_OHM_DIFF	ISL9, ISL10	Y	0.154 MM	0.154 MM		0.200 MM	0.200 MM
72_OHM_DIFF	ISL2, ISL11	Y	0.175 MM	0.175 MM		0.200 MM	0.200 MM
72_OHM_DIFF	TOP, BOTTOM	Y	0.175 MM	0.175 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3, ISL4	Y	0.110 MM	0.110 MM		0.180 MM	0.180 MM
85_OHM_DIFF	ISL9, ISL10	Y	0.110 MM	0.110 MM		0.180 MM	0.180 MM
85_OHM_DIFF	ISL2, ISL11	Y	0.125 MM	0.125 MM		0.190 MM	0.190 MM
85_OHM_DIFF	TOP, BOTTOM	Y	0.125 MM	0.125 MM		0.190 MM	0.190 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3, ISL4	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL9, ISL10	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL2, ISL11	Y	0.115 MM	0.115 MM		0.230 MM	0.230 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.115 MM	0.115 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3, ISL4	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL9, ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2, ISL11	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM
100_OHM_DIFF	TOP, BOTTOM	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3, ISL4	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL9, ISL10	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL2, ISL11	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP, BOTTOM	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.126 MM	?
3X_DIELECTRIC	*	0.189 MM	?
4X_DIELECTRIC	*	0.252 MM	?


NOTE: From T18 MLB, changed to reflect K17 mlb stackup.

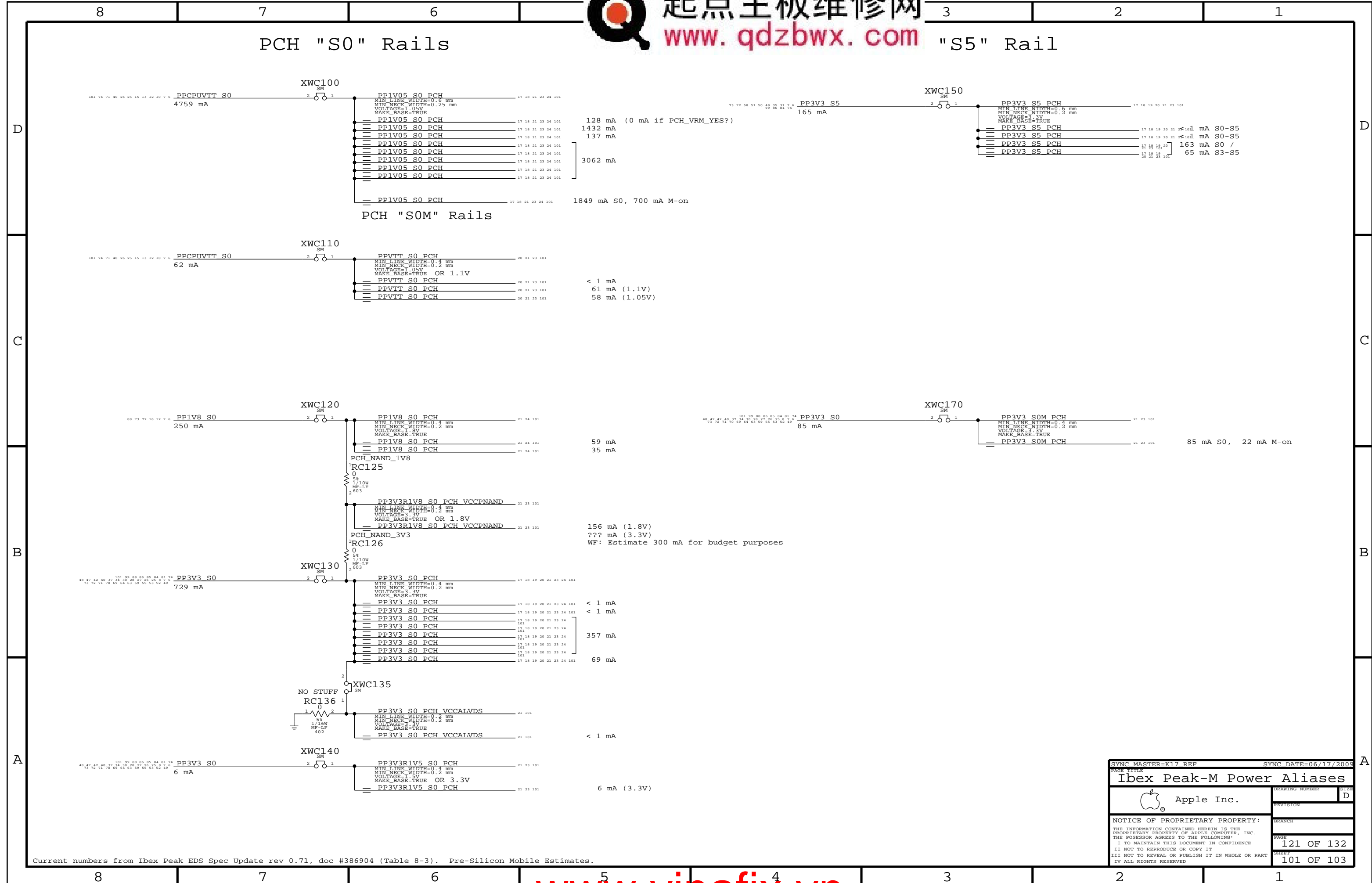
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3, ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9, ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM


NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

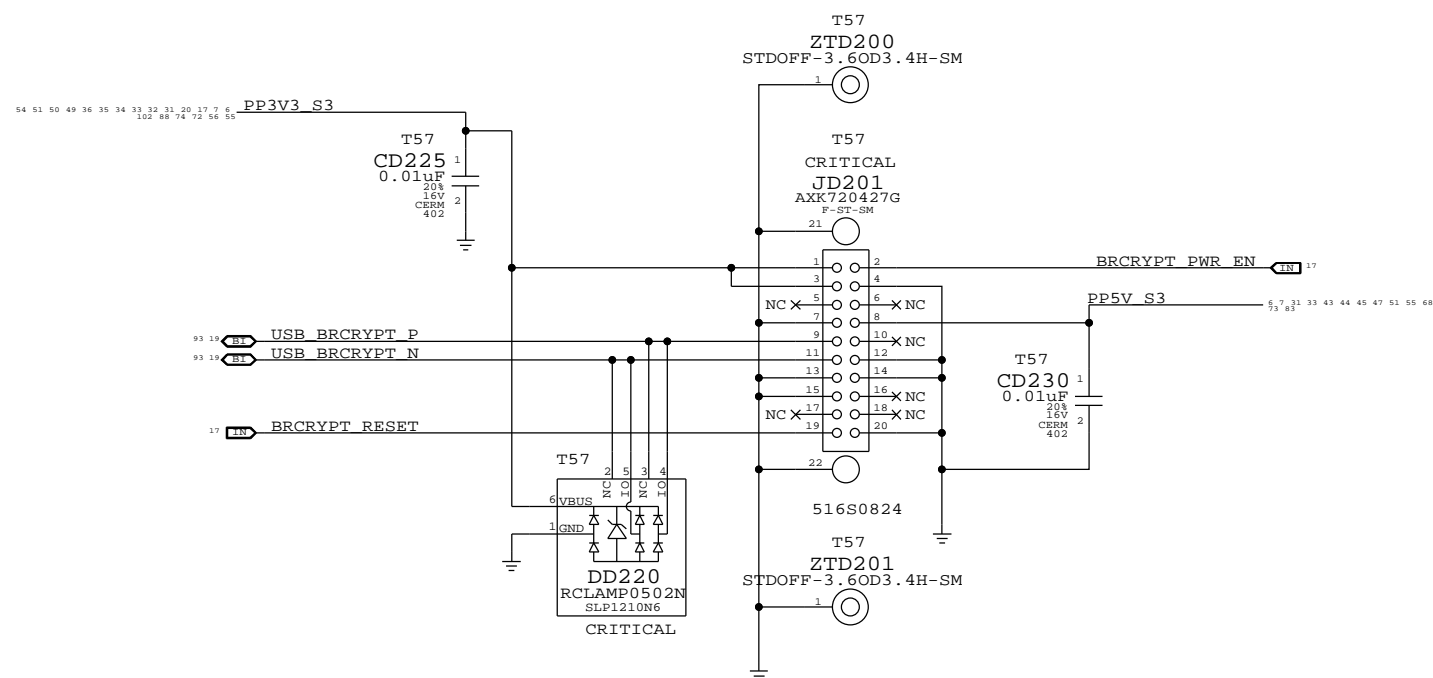
NOTE: 110_DIFF is 110-ohms differential impedance on outer layers and 105-ohms on inner layers.

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